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MS-7A63

Intel -Kabylake plamform Z270

ATX

Ver: 10

CPU:

System Chipset:

kabylake-S

Z270

Onboard Chip:

HD Audio Codec:ALC1220
LAN:INTEL I219
SIO:Nuvoton 6795
Flash ROM: SPI 128MB

Main Memory:

*DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)*

ACPI:

PWM:

NIKO/UPI

UPI9508

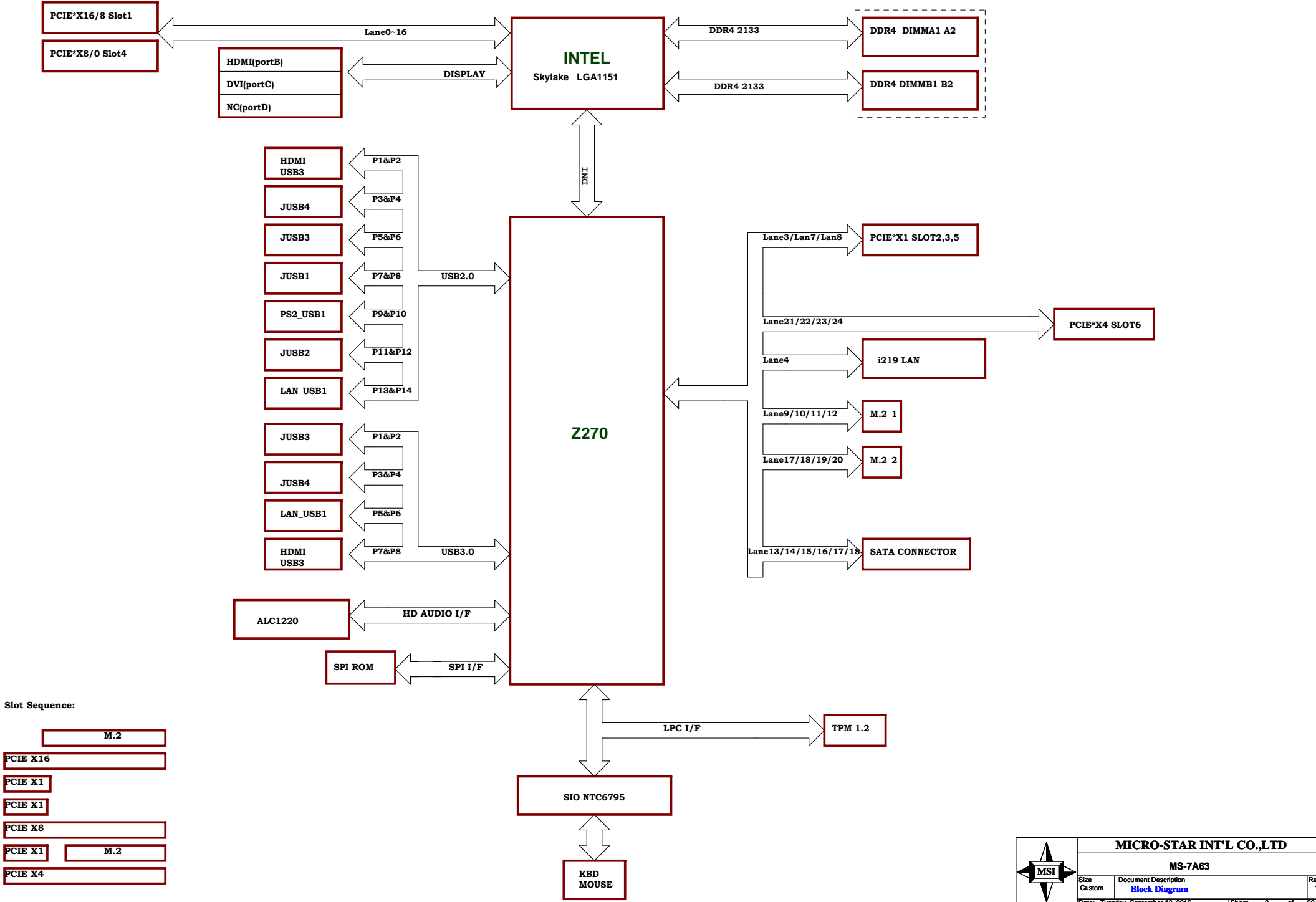
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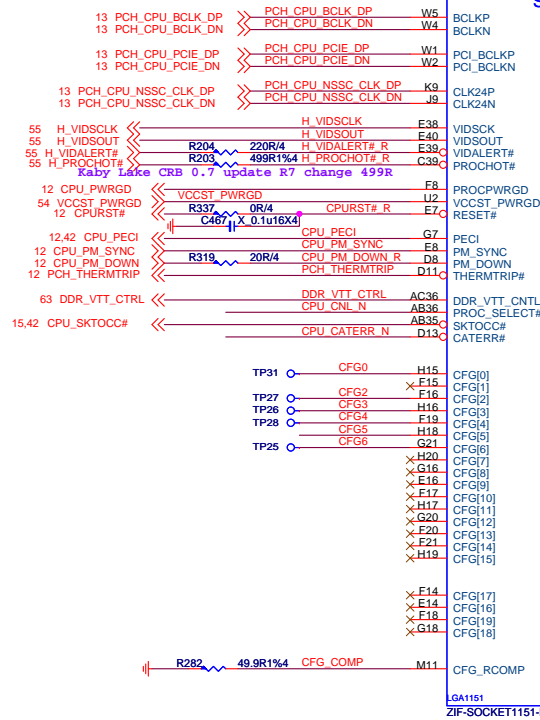
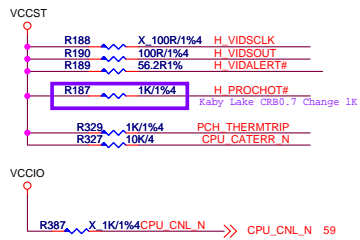
Other:

*PCI Express (X16) Slot *1*
*PCI Express (X8) Slot *1*
*PCI Express (X4) Slot * 1*
*PCI Express (X1) Slot * 3*
*M2 * 2*

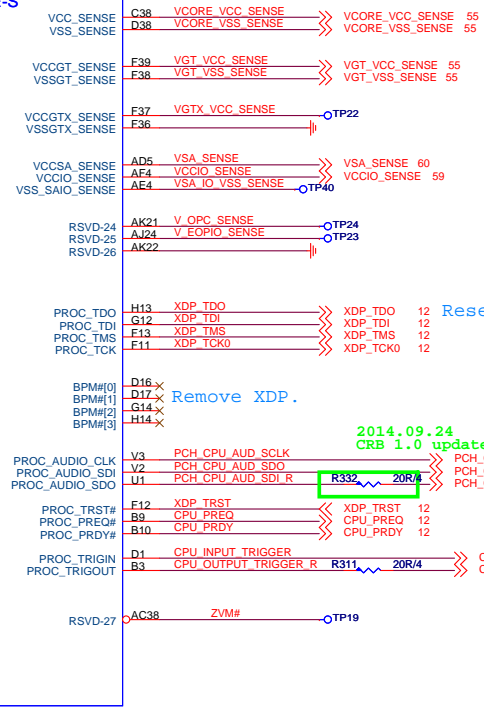
SATA3.0 x6 (PCH)
*FRONT USB2.0 *4*
*FRONTUSB3.0 *4*
*REAR USB3.0 *4*
*REAR USB2.0 *2*
REAR USB TYPE A+C

MS-7A63 Block Diagram





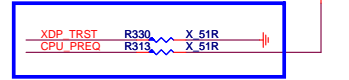
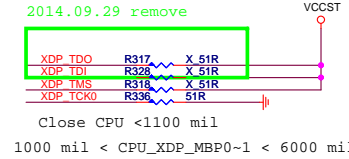
SKYLAKE-S



CFG Strap

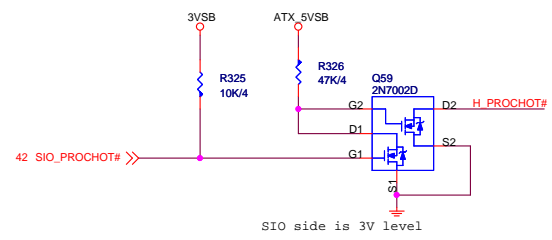
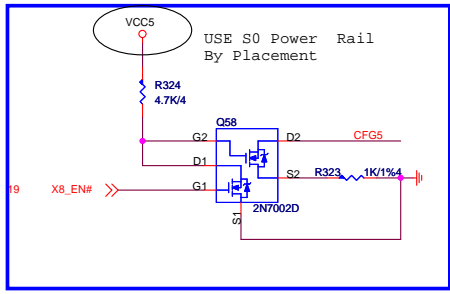
CFG Table			
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

Reserve for DCI.



x8 Ctrl

ENABLE#	SLOT1	SLOT4
X8		
0	X8	X8
1	X16	X0

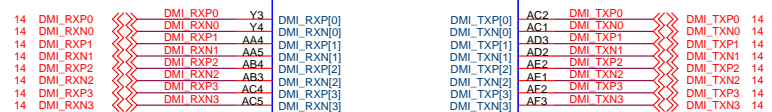
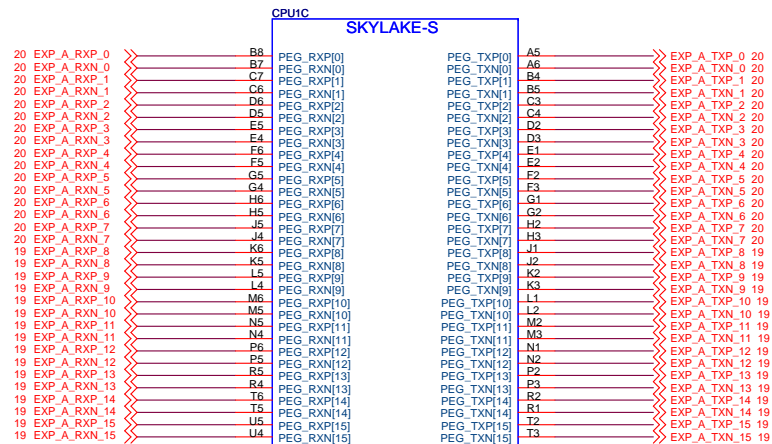


CFG Strap

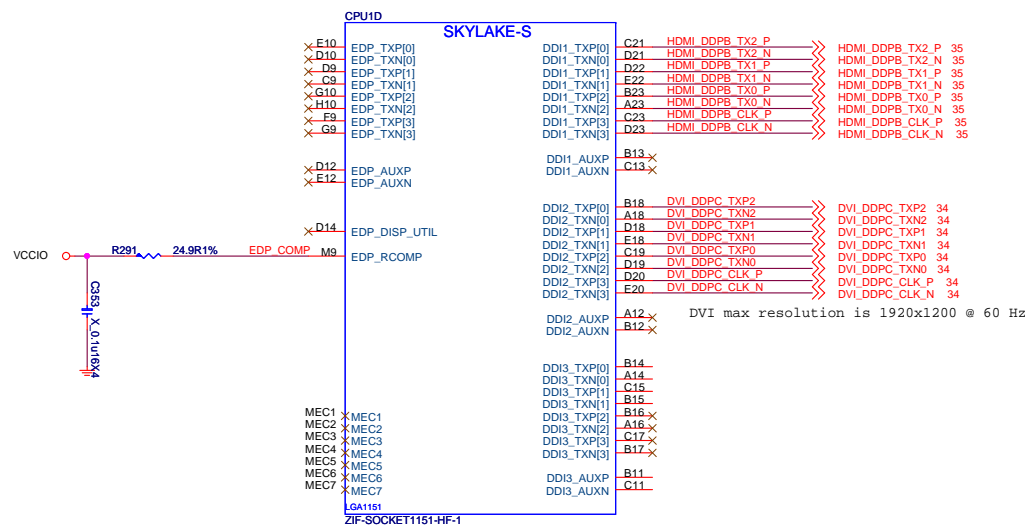
CFG Table			
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		



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MS-7A63			
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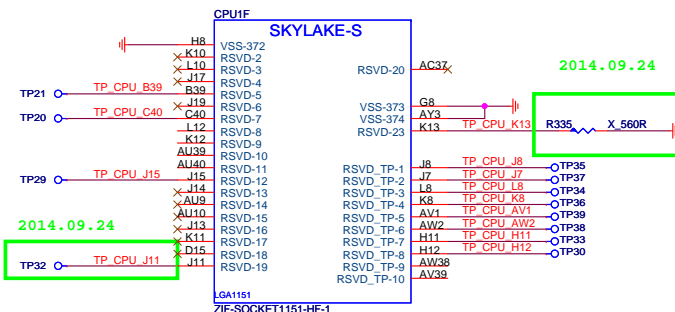


LGA1151 ZIF-SOCKET1151-HF-1

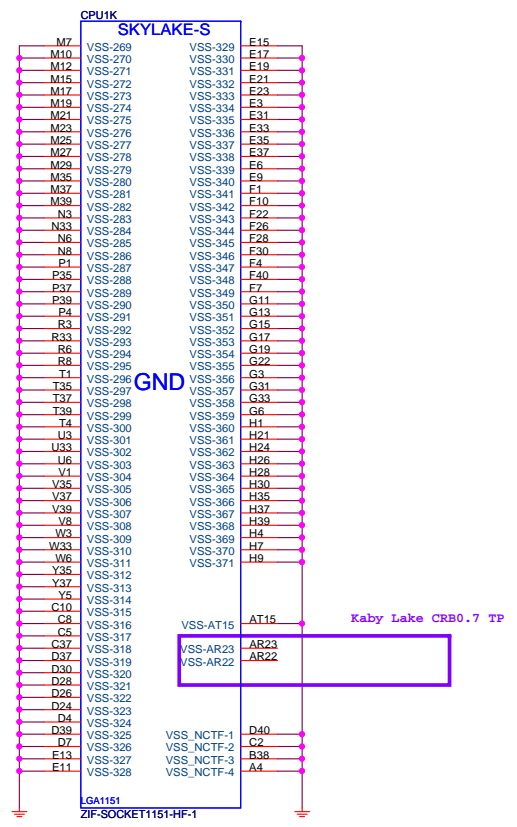
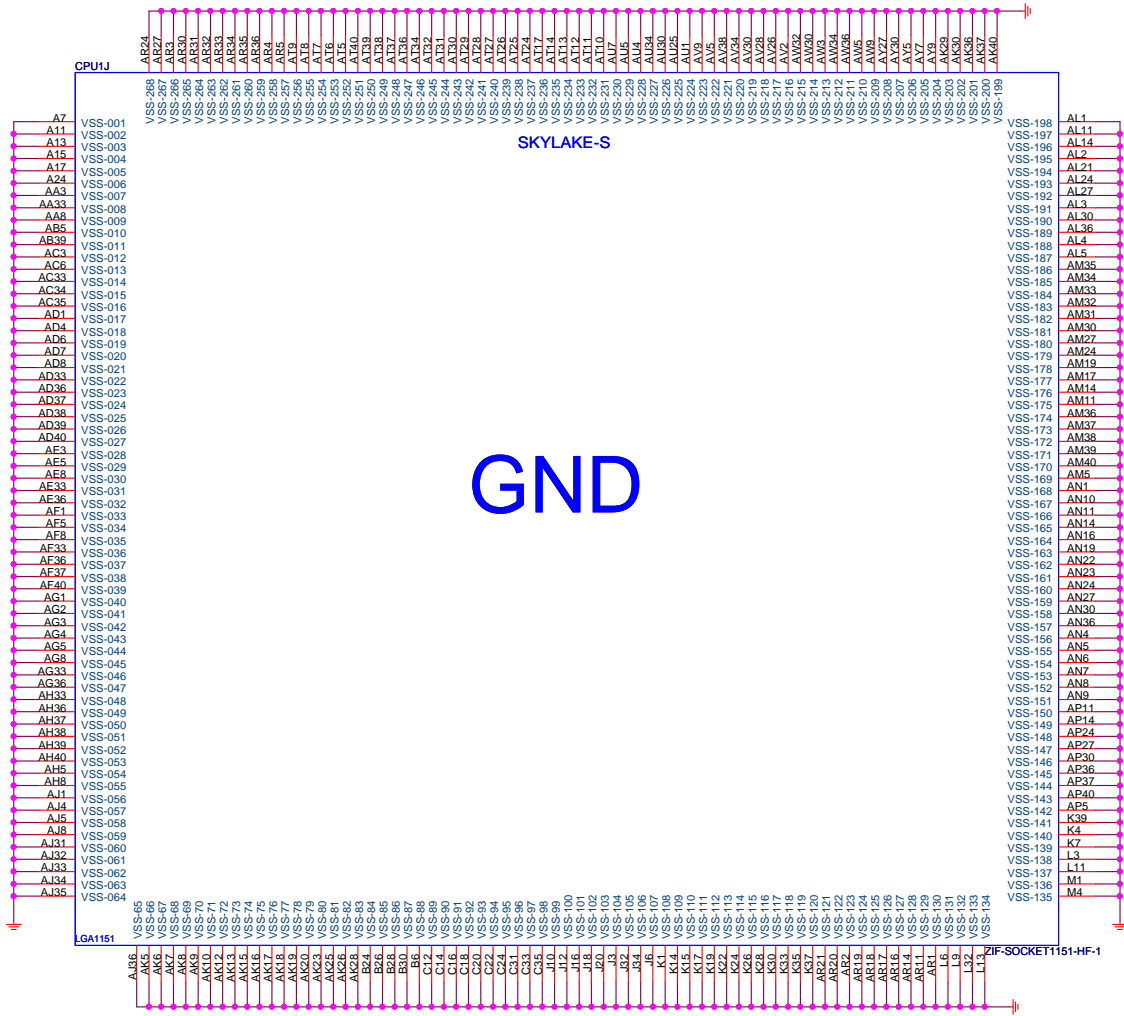


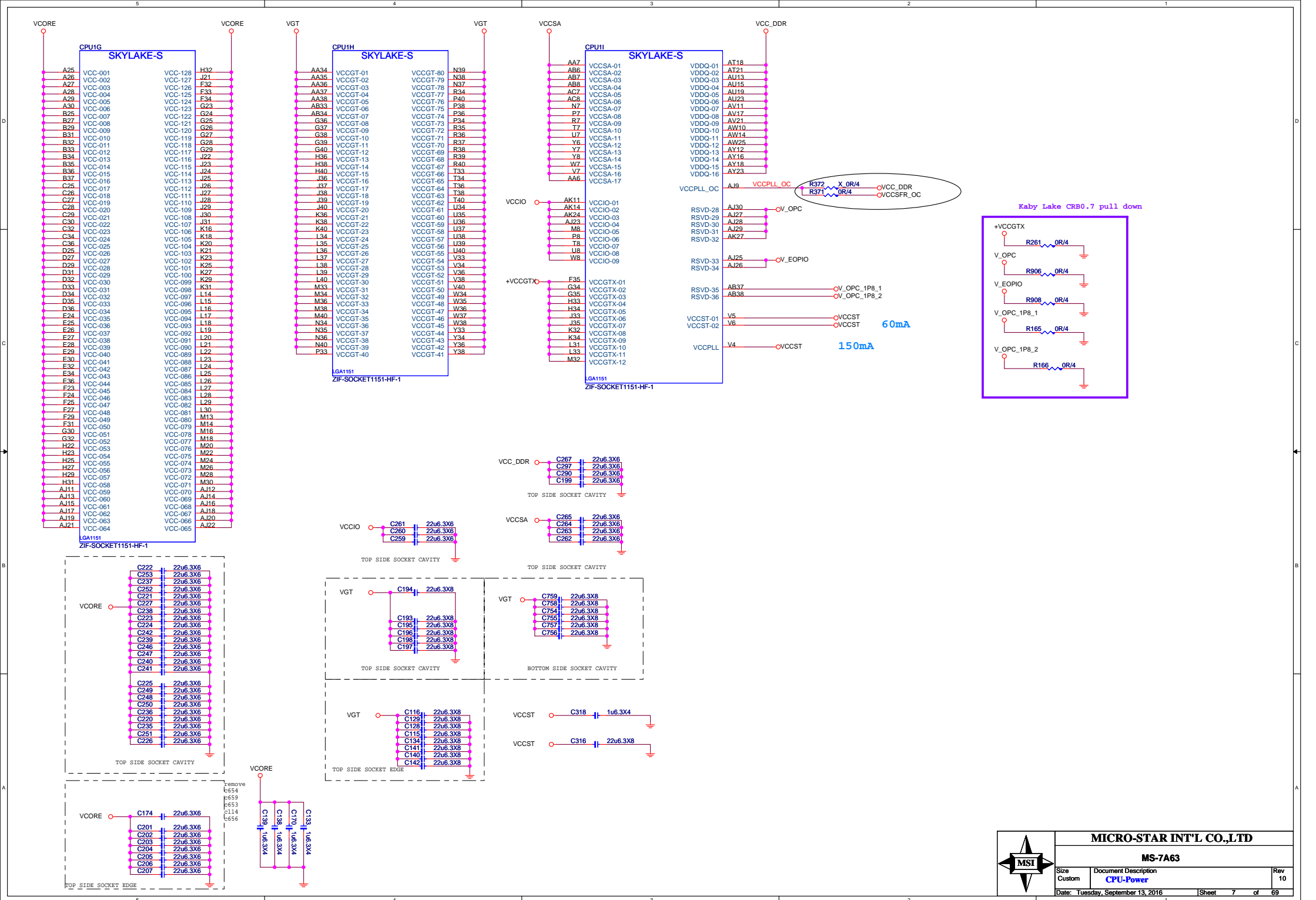
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MEC2
MEC3
MEC4
MEC5
MEC6
MEC7

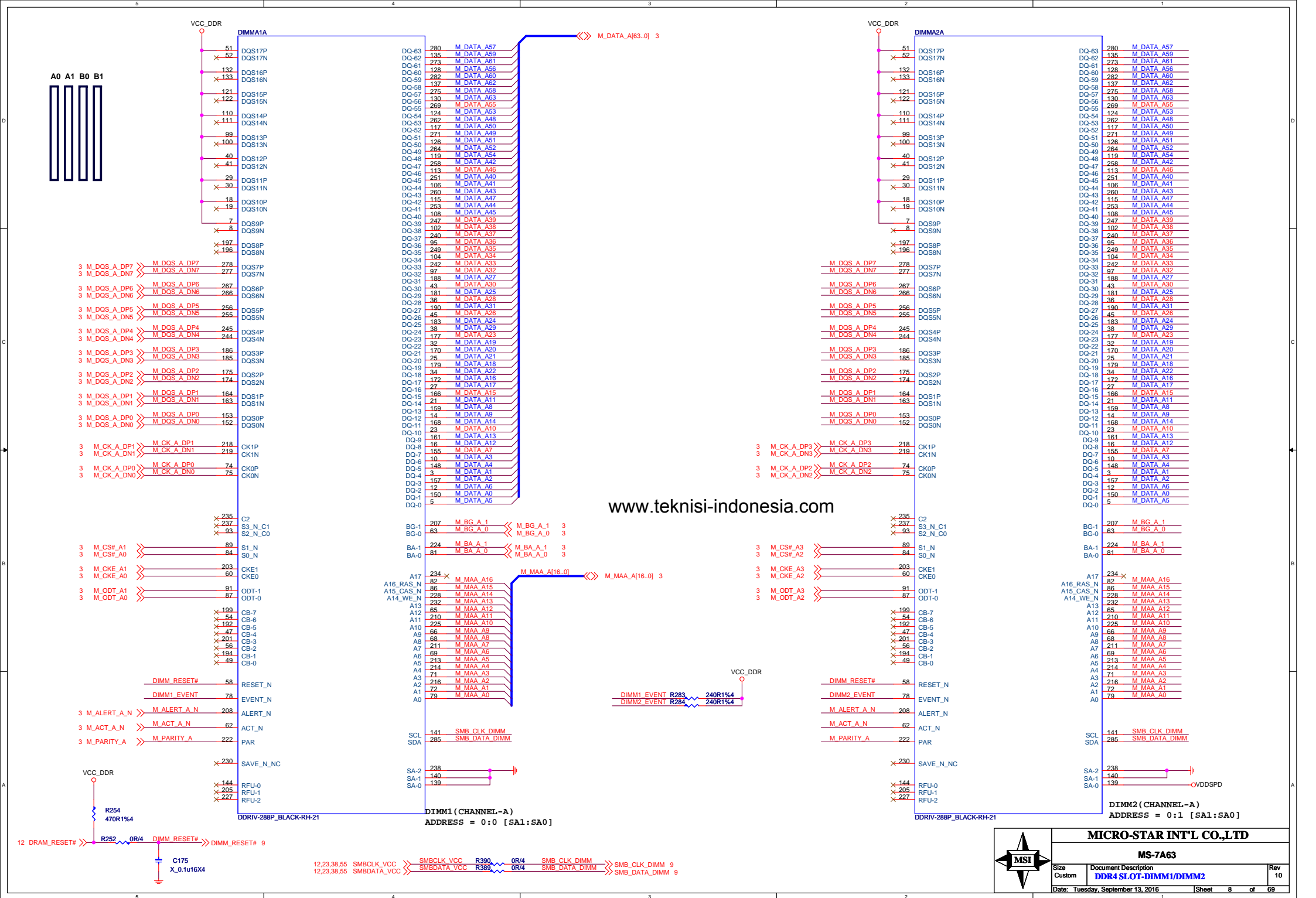
LGA1151 ZIF-SOCKET1151-HF-1



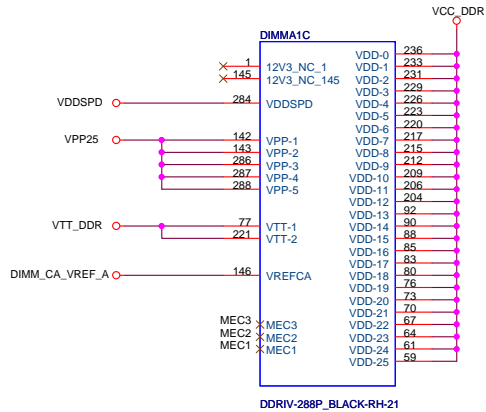
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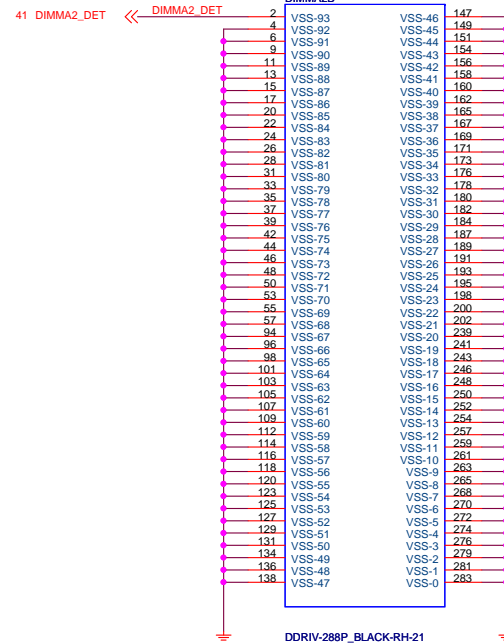
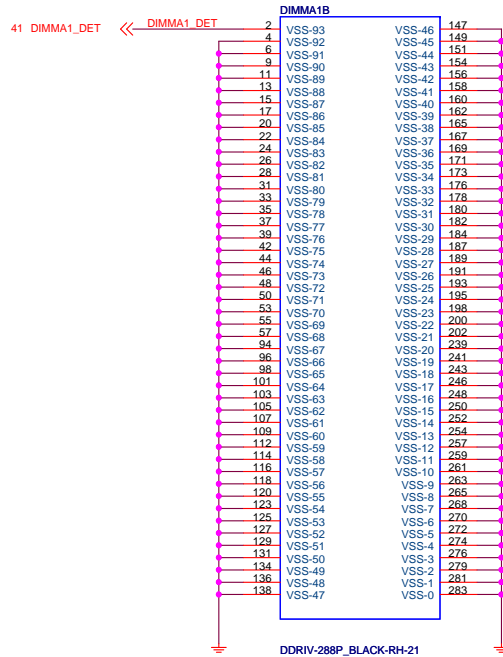
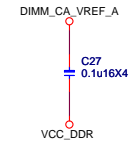
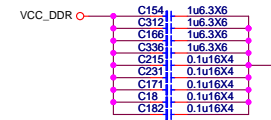
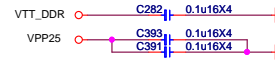
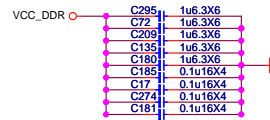
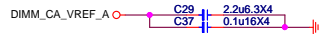
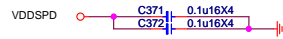
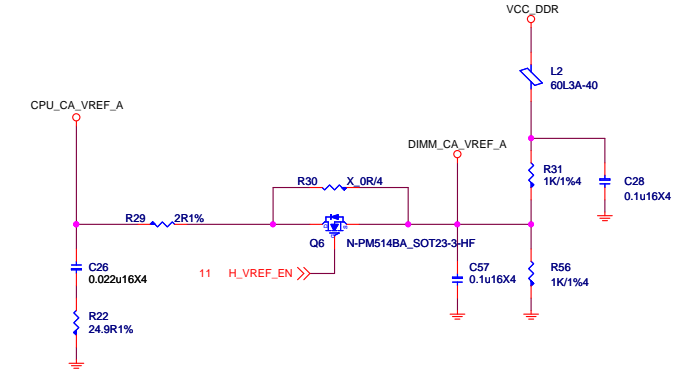
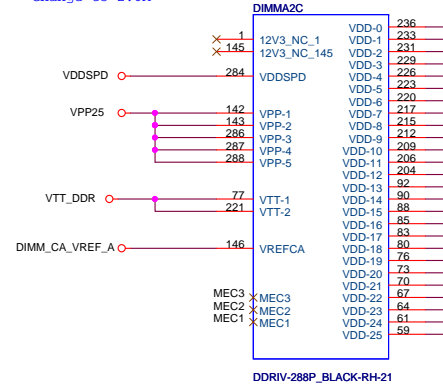
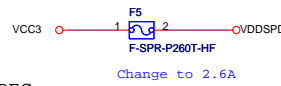
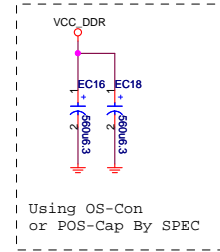




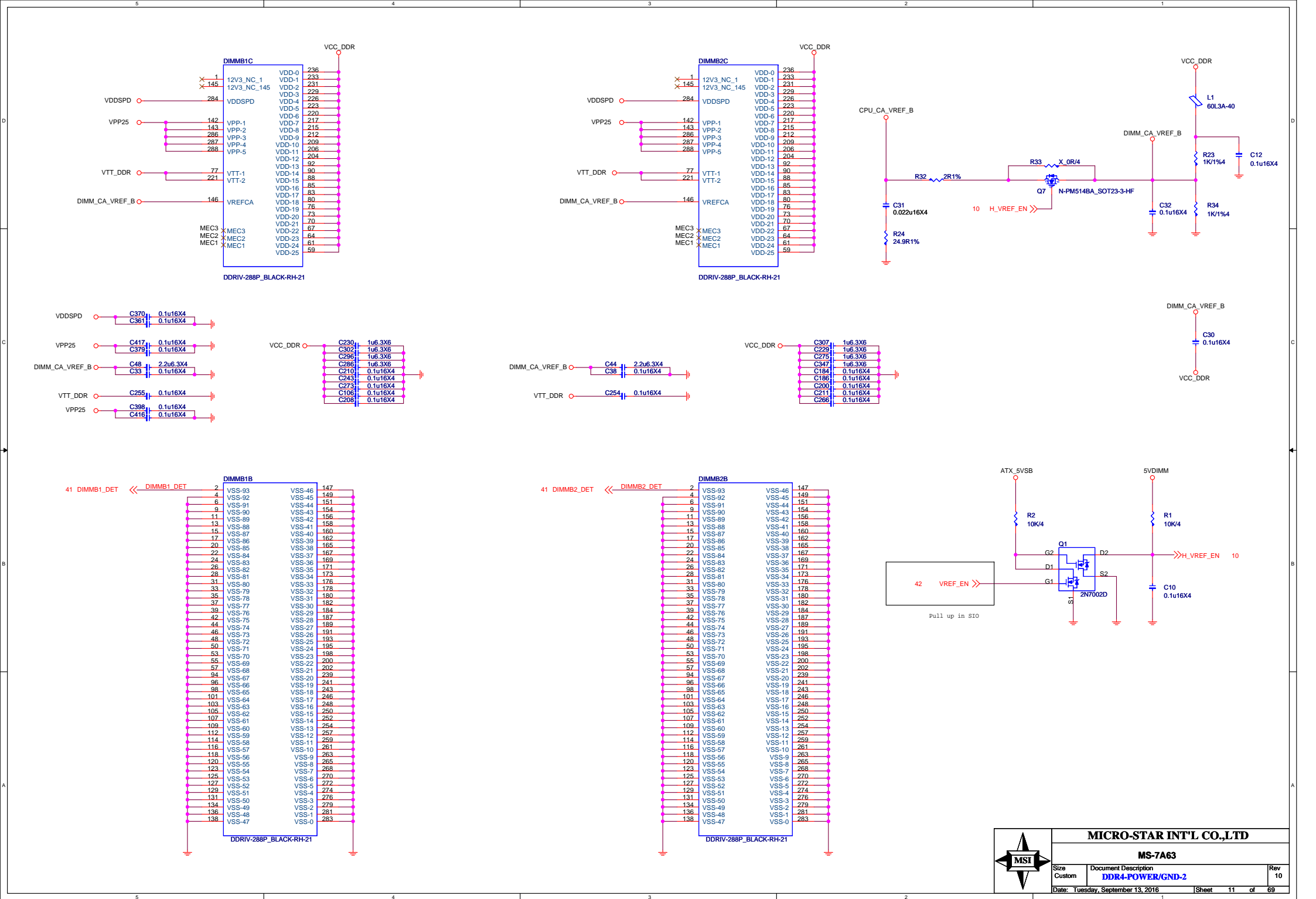
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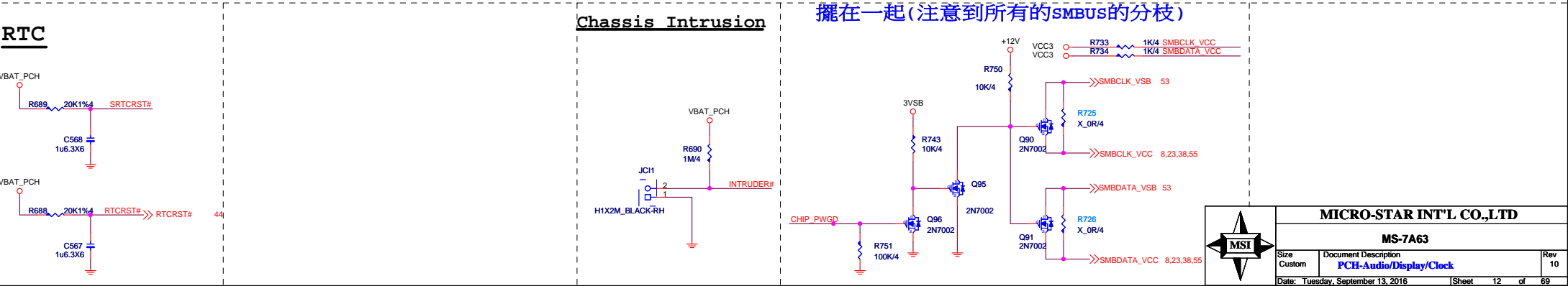
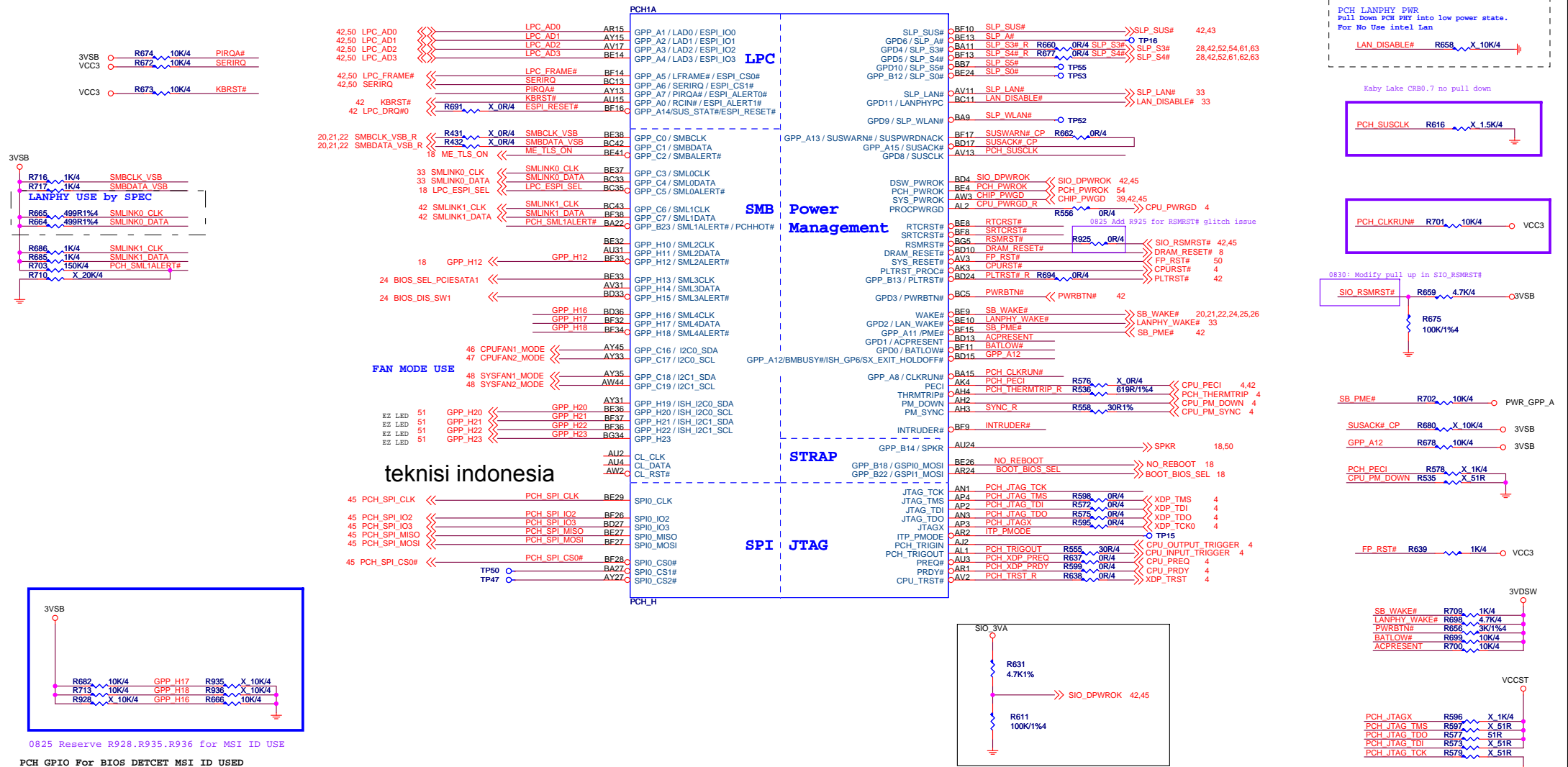


DIMM SLOT PN BY SPEC



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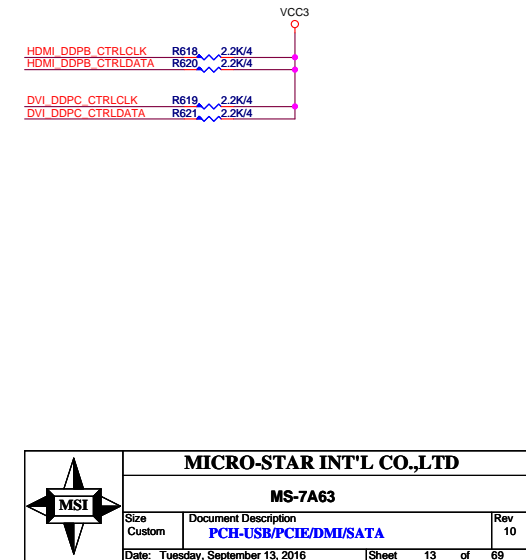
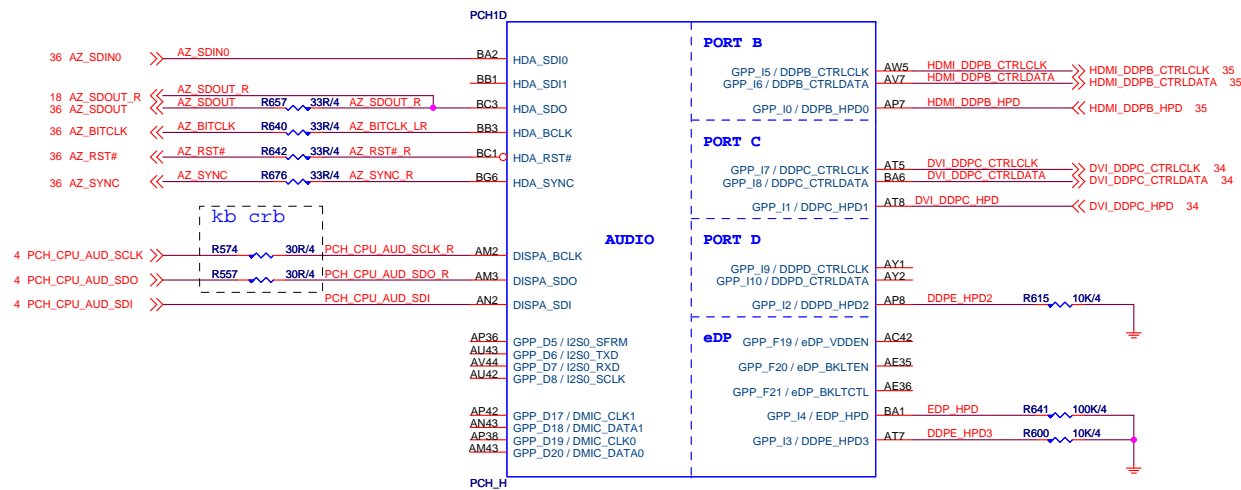
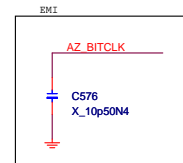
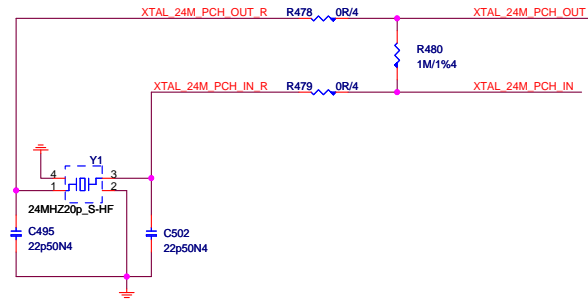
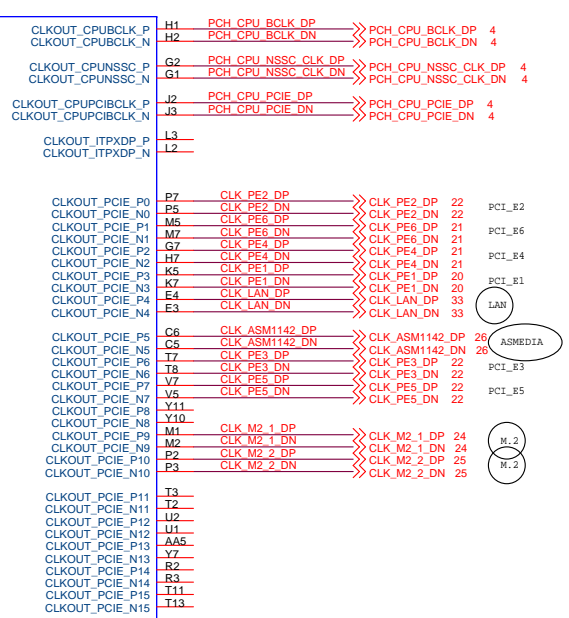
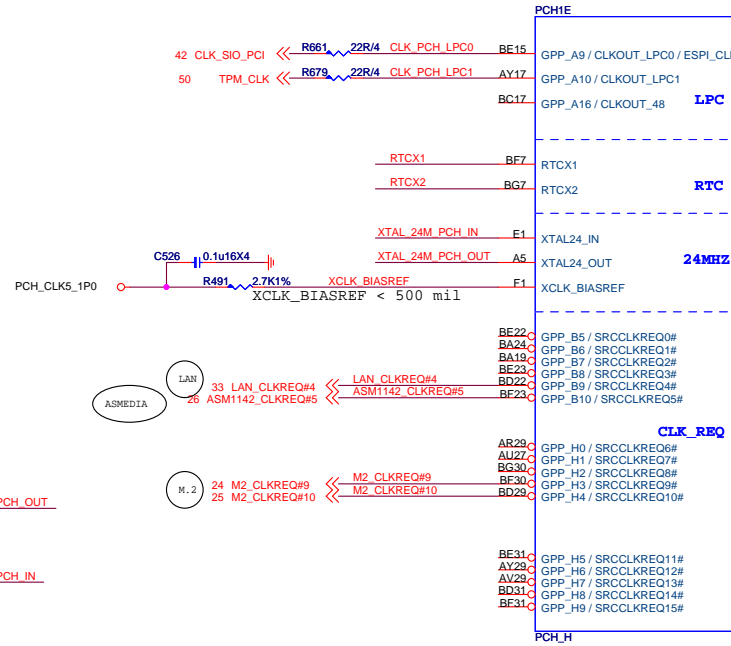
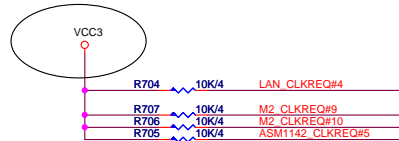
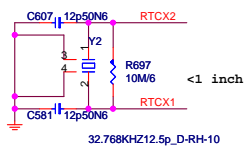


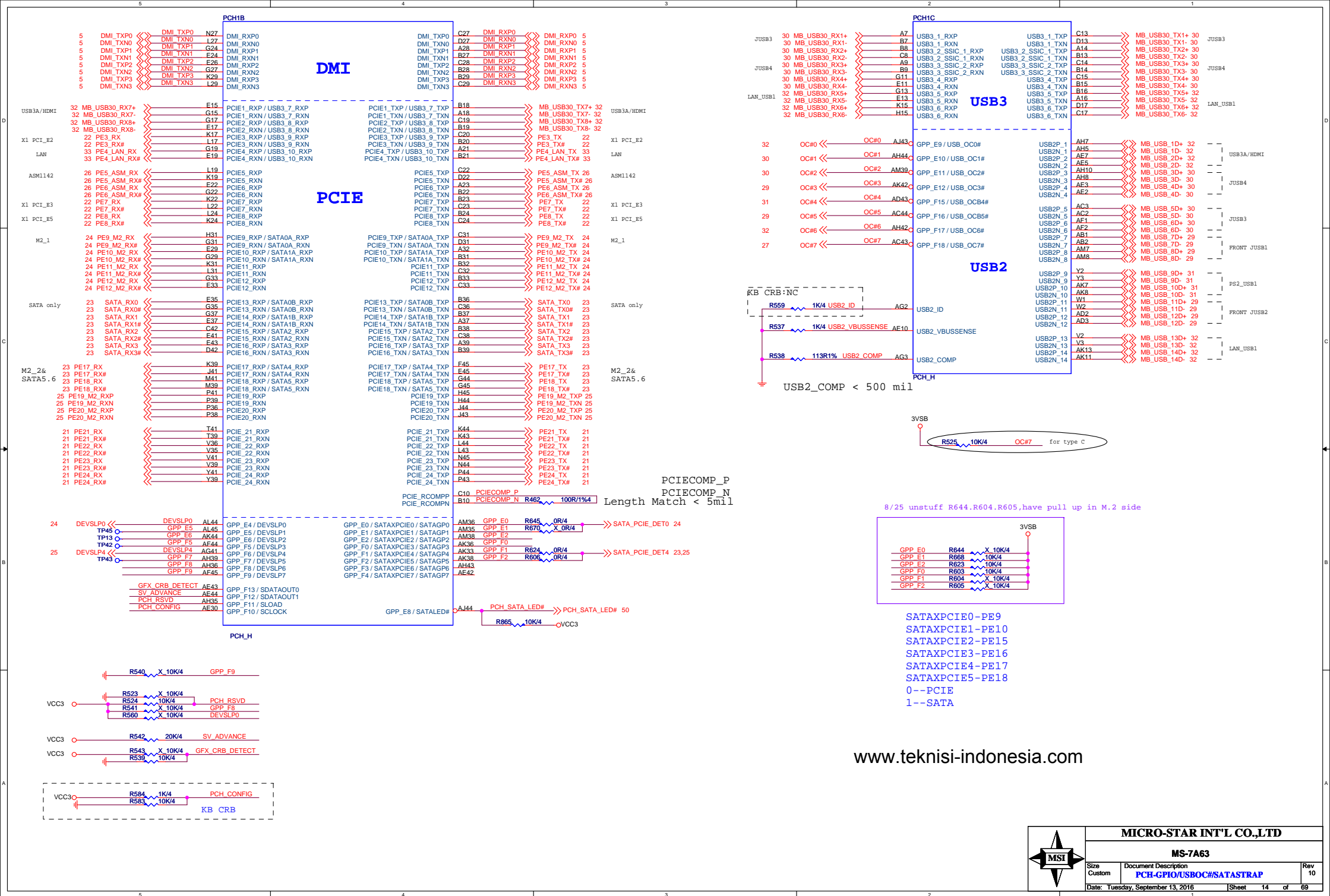


PCH_CLK

RTC Block

Close to PCH





D

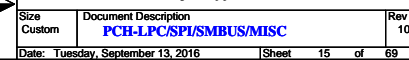
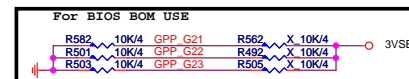
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B

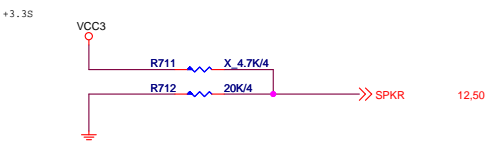


1



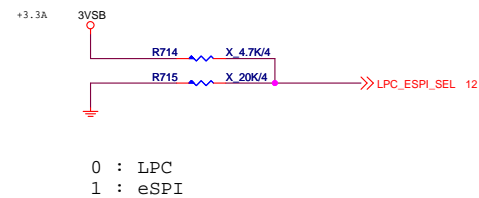
VSS

TOP Swap



Internal pull-down is disabled after PLTRST#

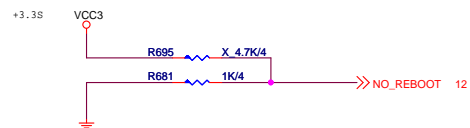
LPC eSPI Mode



Internal pull-down is disabled after RSMRST

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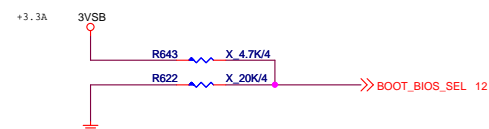
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

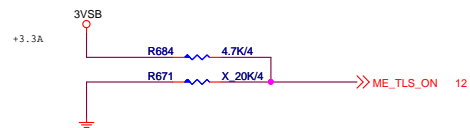
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

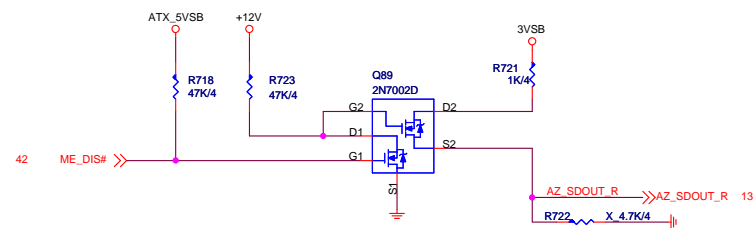
AMT and SBA with confidentiality



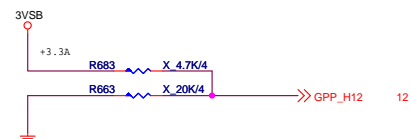
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE

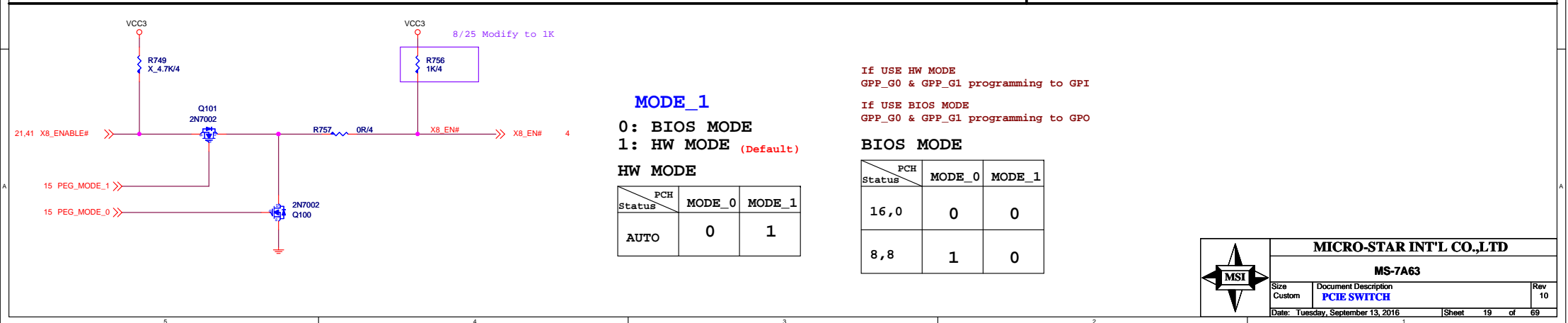
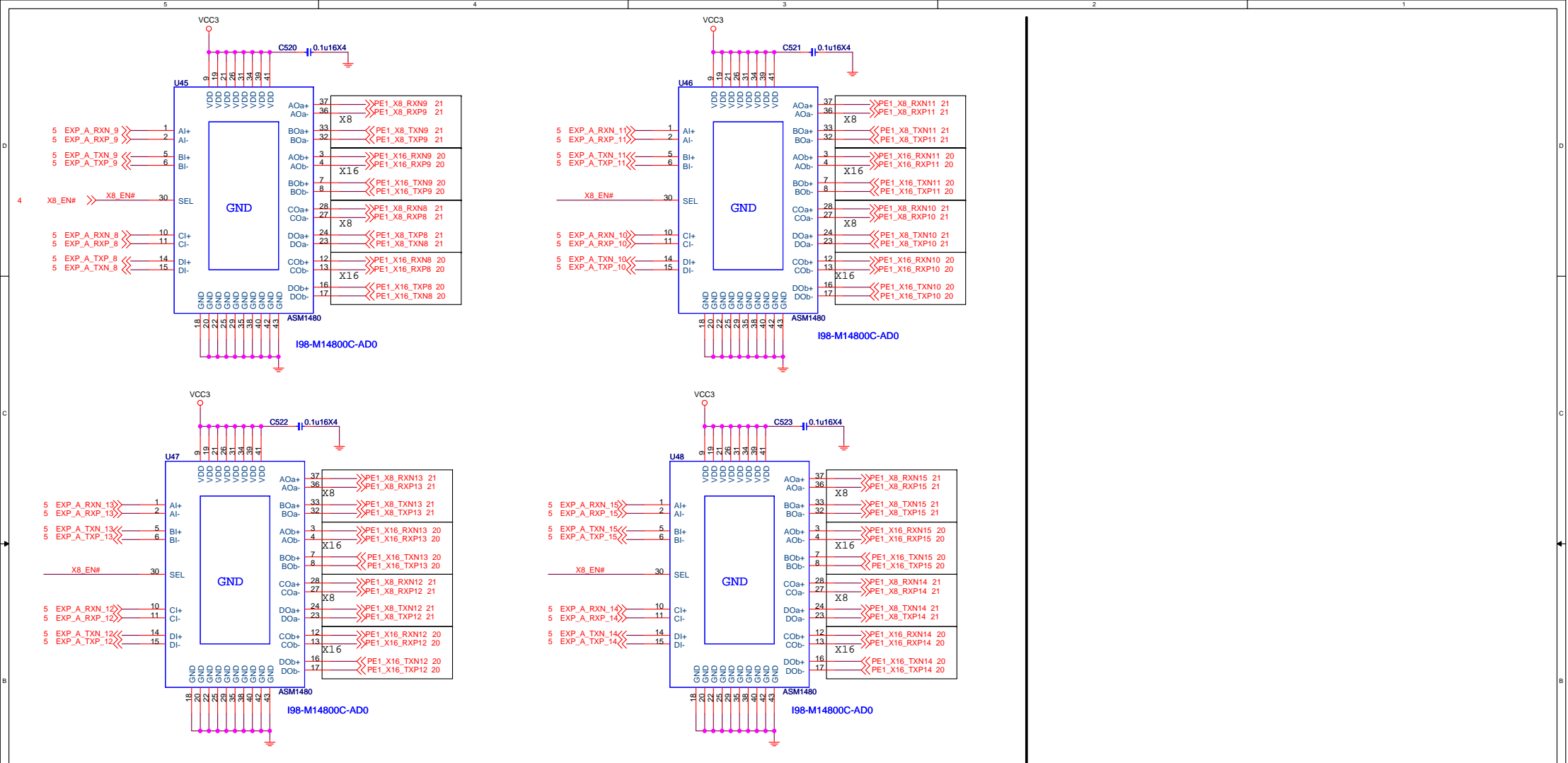


0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down is disabled after RSMRST



MICRO-STAR INT'L CO.,LTD		
MS-7A63		
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MODE_1

0: BIOS MODE
1: HW MODE (Default)

HW MODE

PCH Status	MODE_0	MODE_1
AUTO	0	1

If USE HW MODE
GPP_G0 & GPP_G1 programming to GPI

If USE BIOS MODE
GPP_G0 & GPP_G1 programming to GPO

BIOS MODE

PCH Status	MODE_0	MODE_1
16,0	0	0
8,8	1	0



MICRO-STAR INT'L CO.,LTD

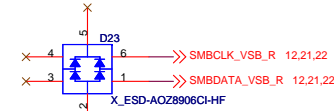
MS-7A63

Size	Document Description	Rev
Custom	PCIE SWITCH	10
Date: Tuesday, September 13, 2016	Sheet 19 of 69	

12V - 5.5A
VCC3 - 3A
3VSBV - 375mA

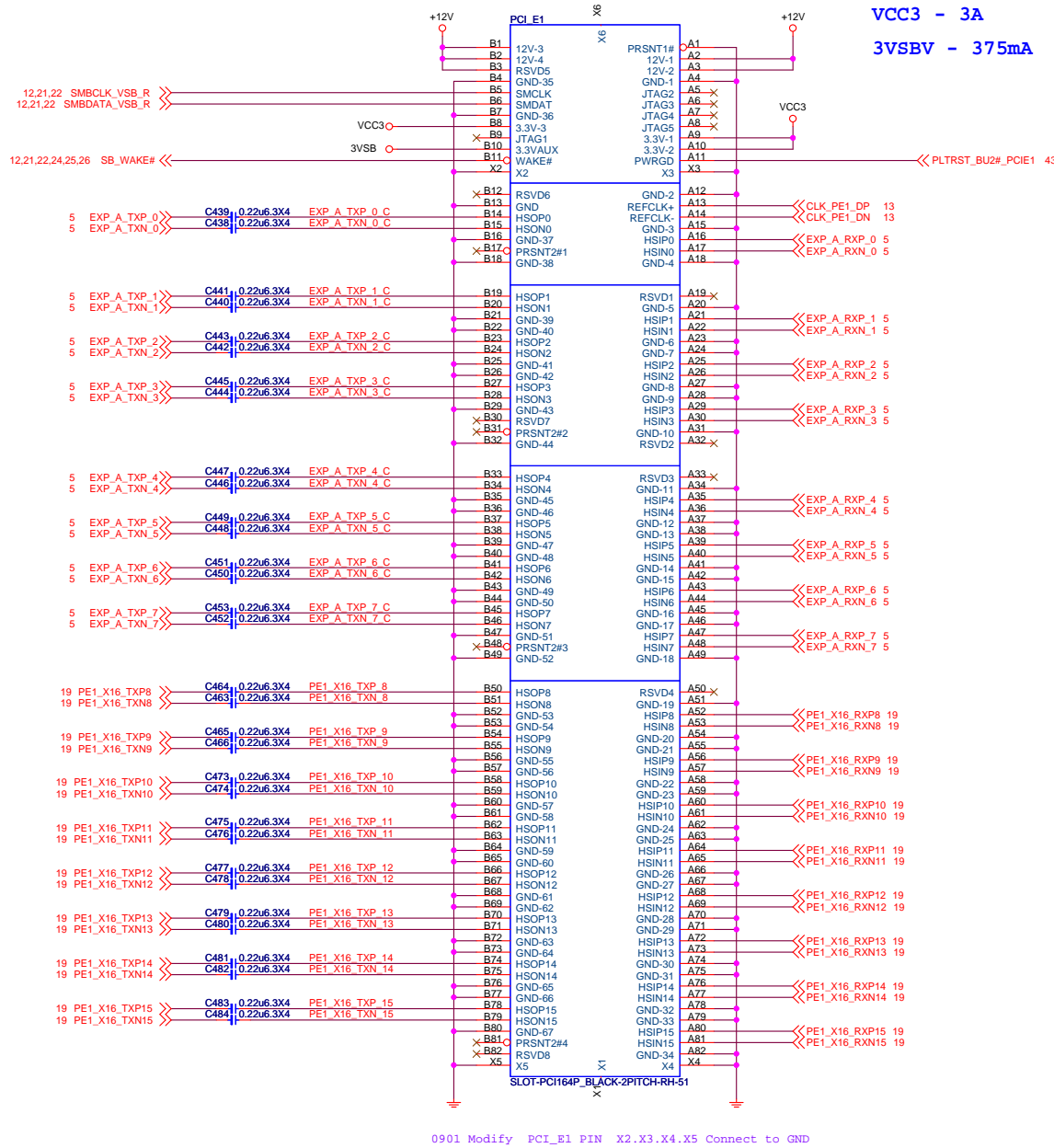
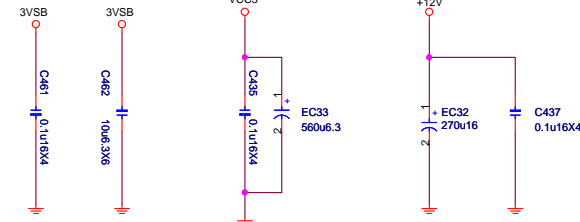
SMBUS ESD

SMBCLK_VSB_R R435 4.7K/4
SMBDATA_VSB_R R436 4.7K/4



By Placement

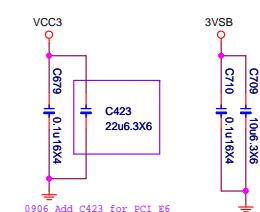
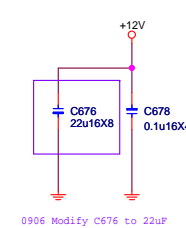
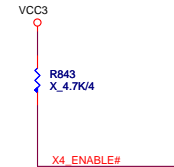
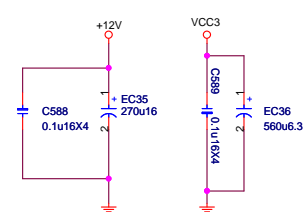
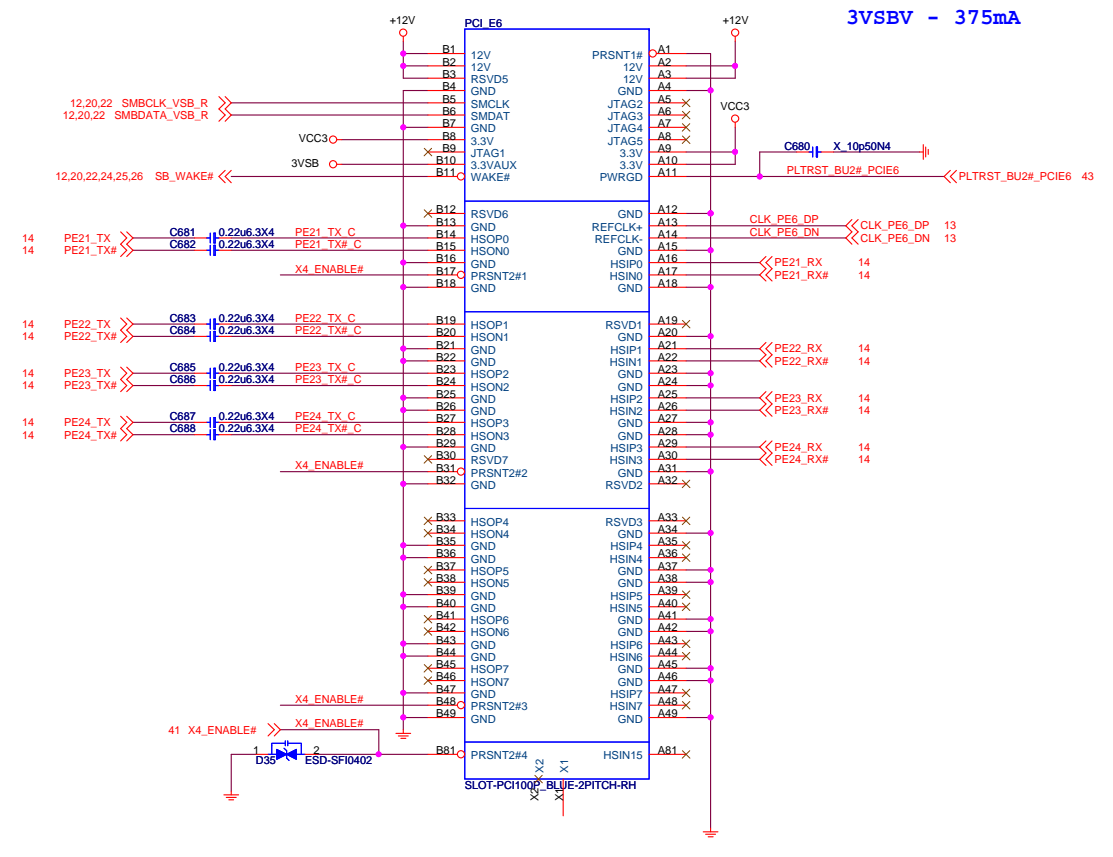
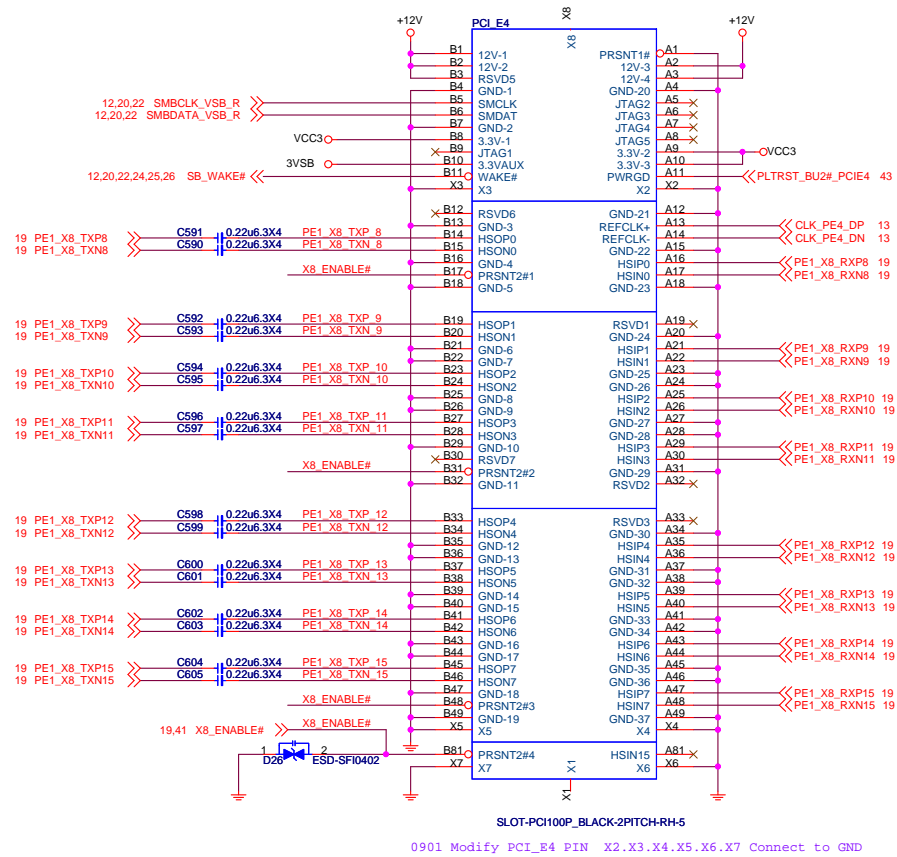
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AVL:D0G-45B0510-I14



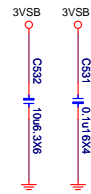
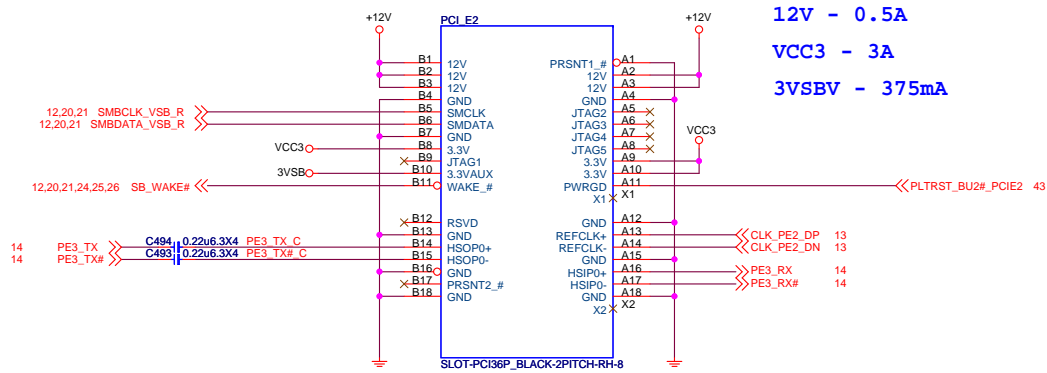
0901 Modify PCI_E1 PIN X2.X3.X4.X5 Connect to GND

PCI_Express X4 Slot

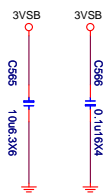
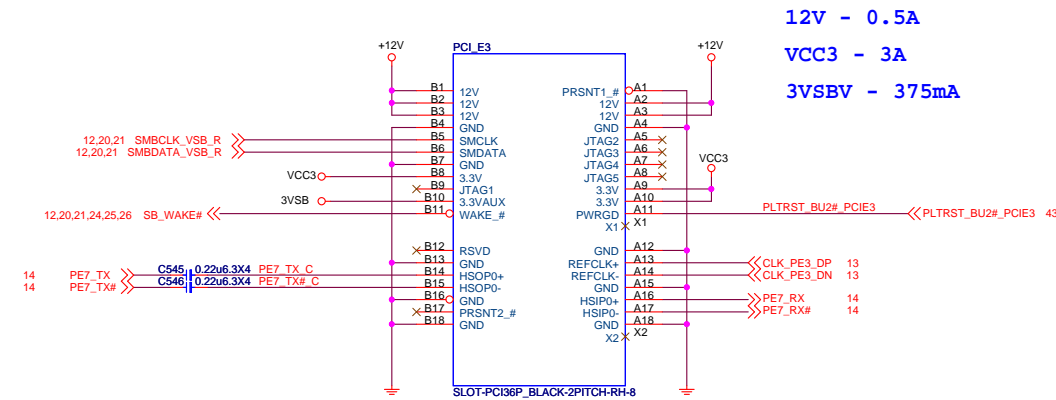
12V - 2.1A
VCC3 - 3A
3VSBV - 375mA



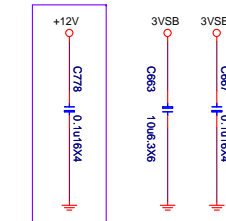
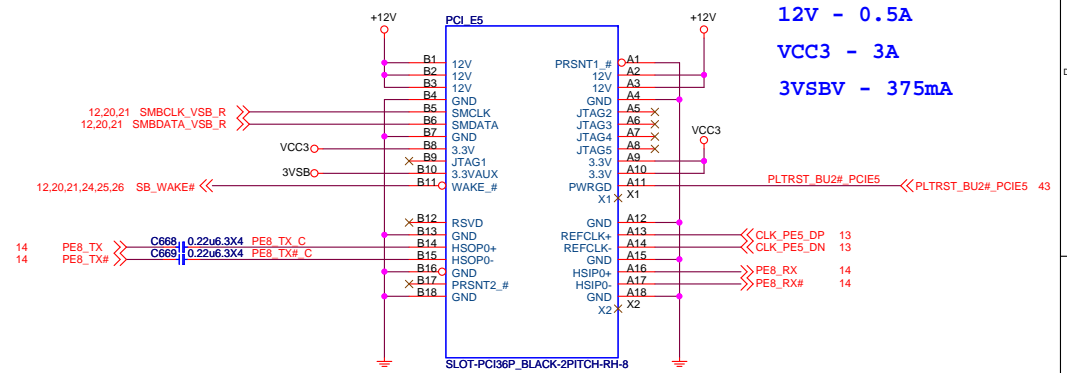
2016.08.25 Modify to N11-0360211-F02



2016.08.25 Modify to N11-0360211-F02

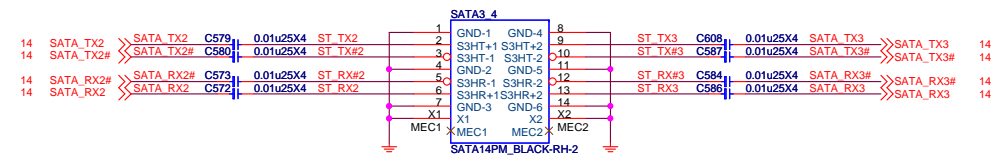
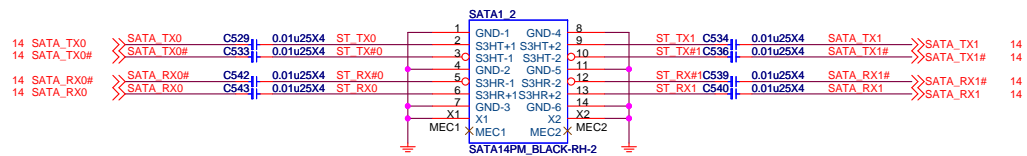


2016.08.25 Modify to N11-0360211-F02

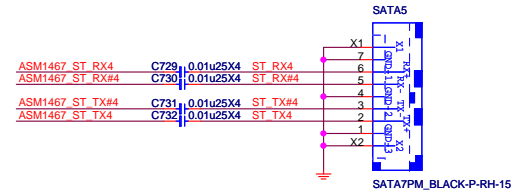
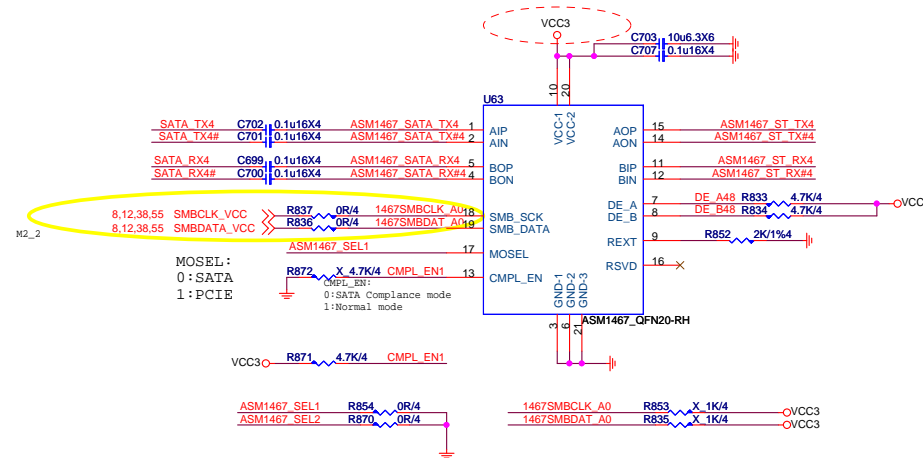
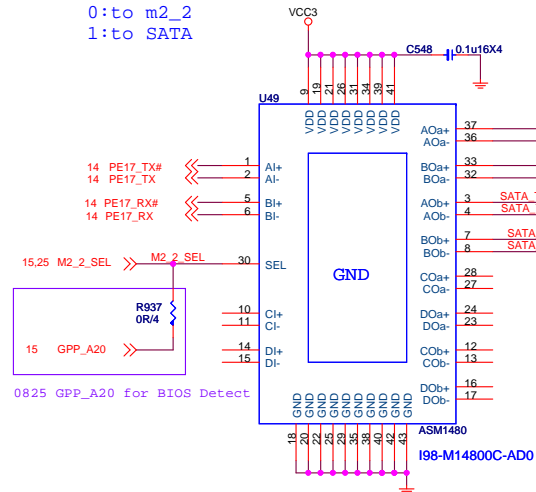


0905 Add C778

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MS-7A63			
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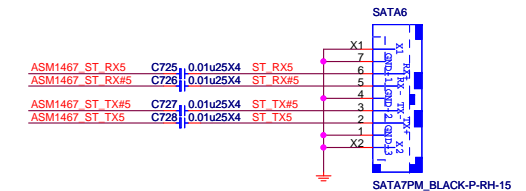
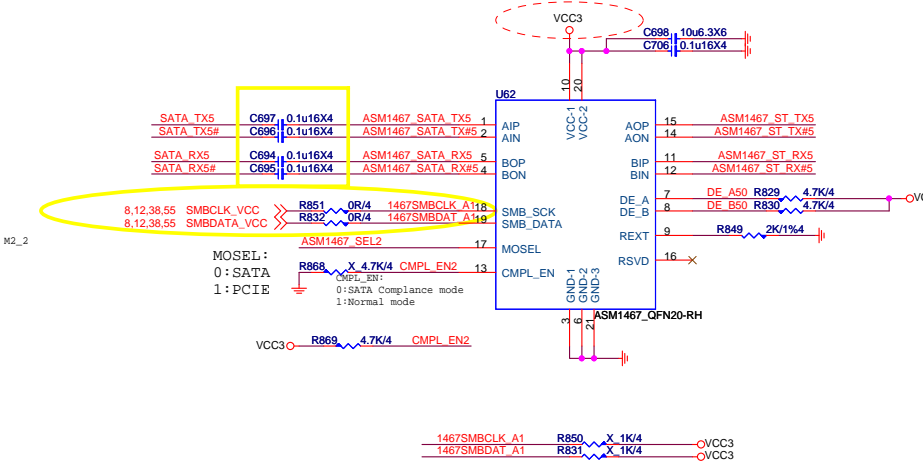
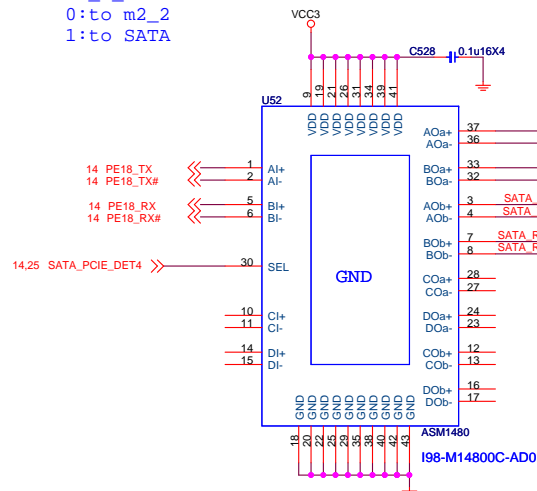


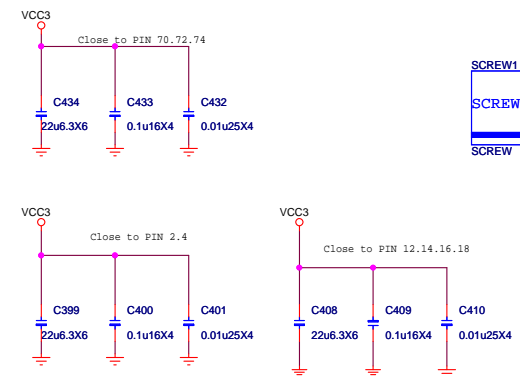
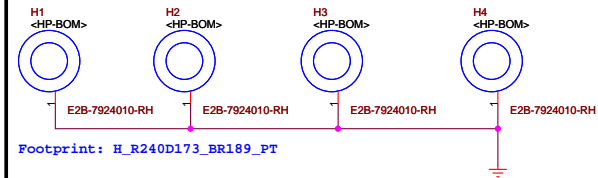
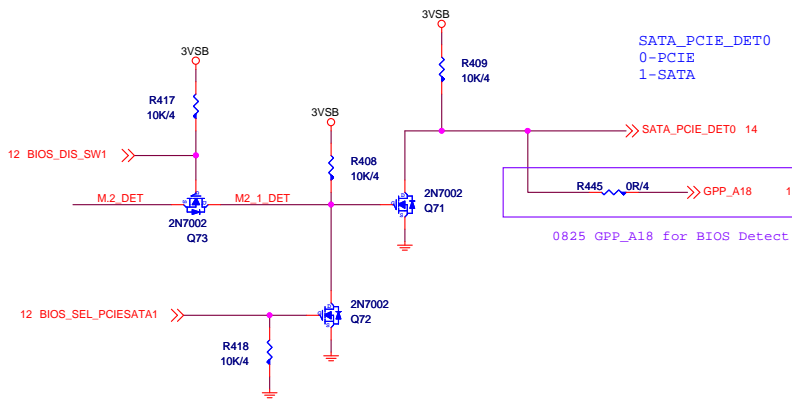
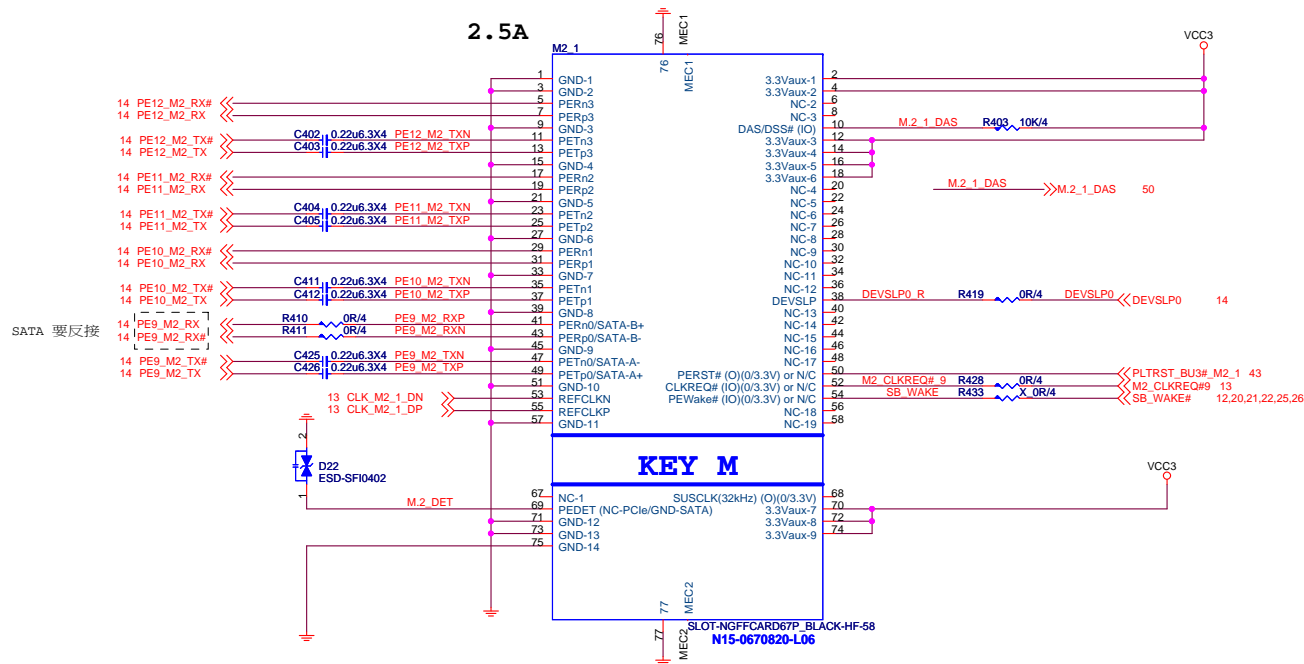
M2_2_SEL
 0:to m2_2
 1:to SATA



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M2_2_SEL
 0:to m2_2
 1:to SATA



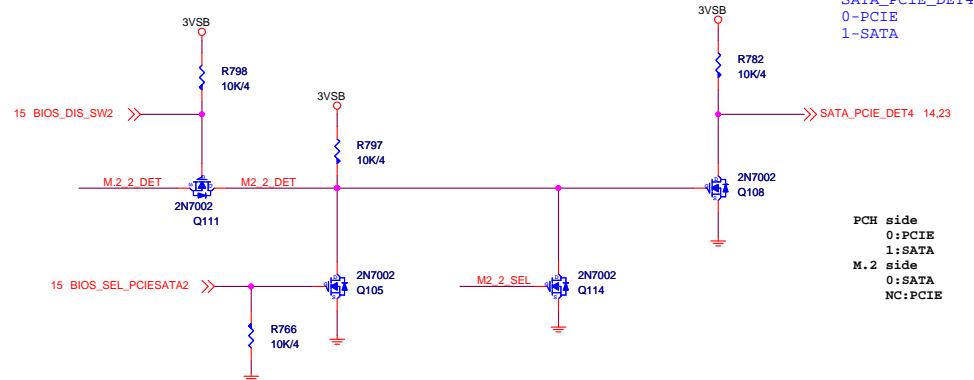
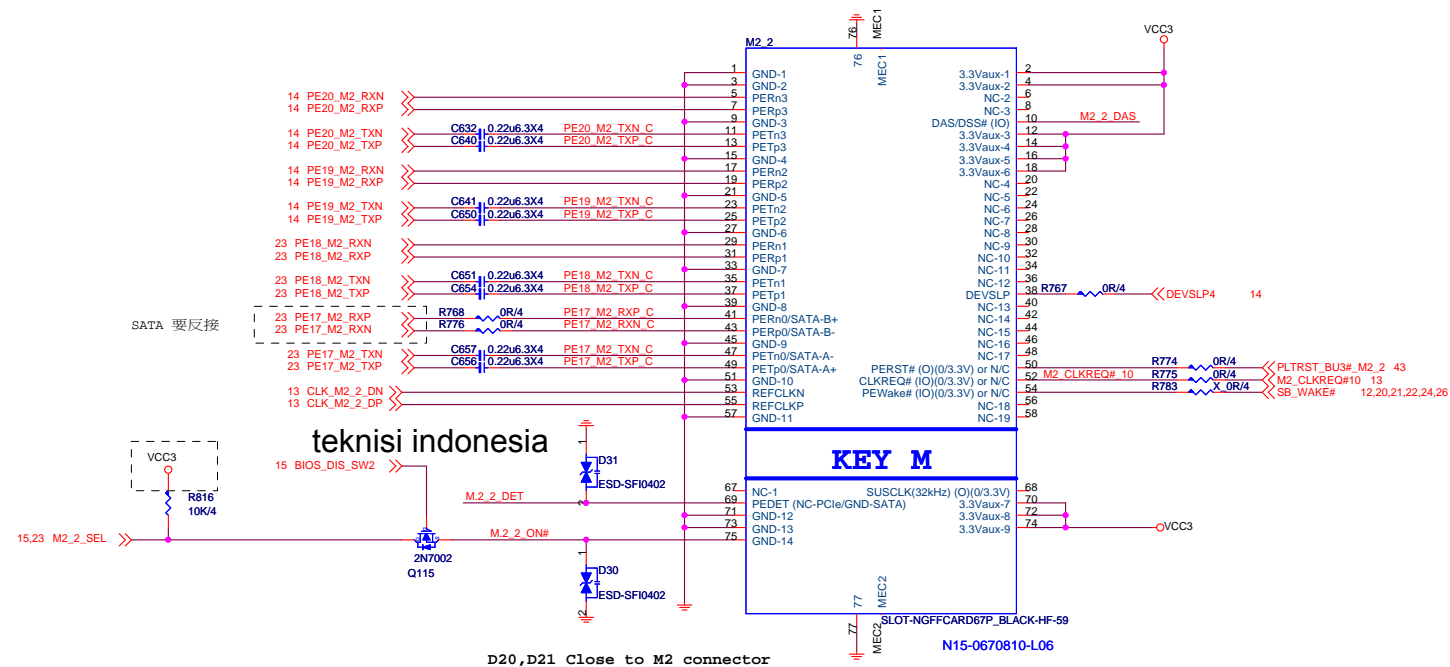
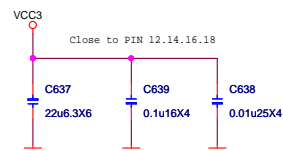
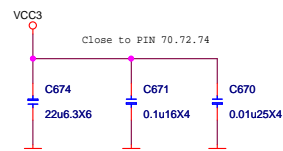
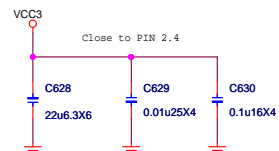


BIOS_MODE

GPP_H15

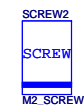
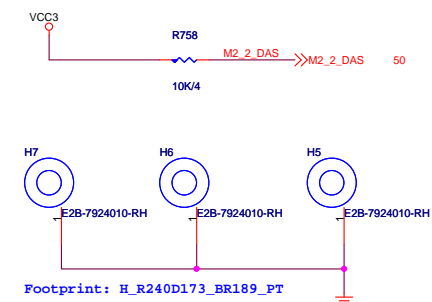
GPP_H13

BIOS_DIS_SW1	BIOS_SEL_PCIESATA1	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI	GPI	AUTO



BIOS_MODE

GPP_G7	GPP_G6	GPP_G5	
<i>BIOS_DIS_SW</i>	<i>M2_2_SEL</i>	<i>BIOS_SEL_PCIESATA2</i>	<i>Mode</i>
<i>GPI(1)</i>	<i>GPI(1)</i>	<i>GPI(0)</i>	<i>AUTO</i>
0	1	0	SATA5
0	0	1	M2-SATA
0	0	0	M2-PCIE

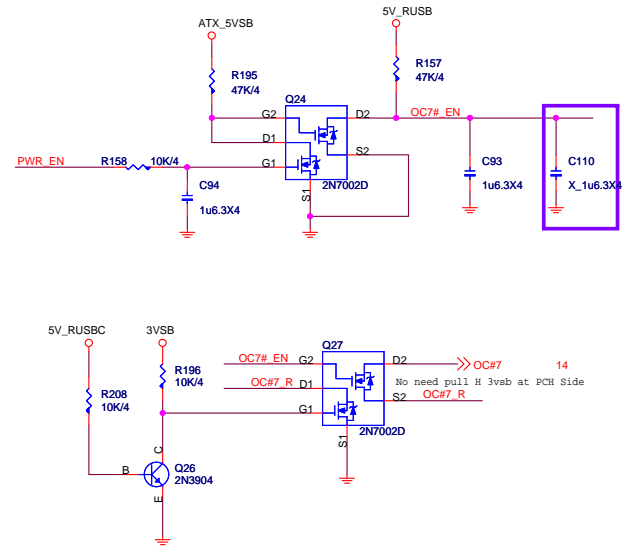


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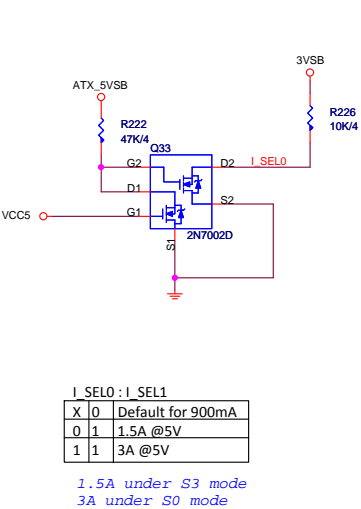
MS-7A63

Size Custom	Document Description M.2-SLOT2	Rev 10
Date: Tuesday, September 13, 2016		Sheet 25 of 69

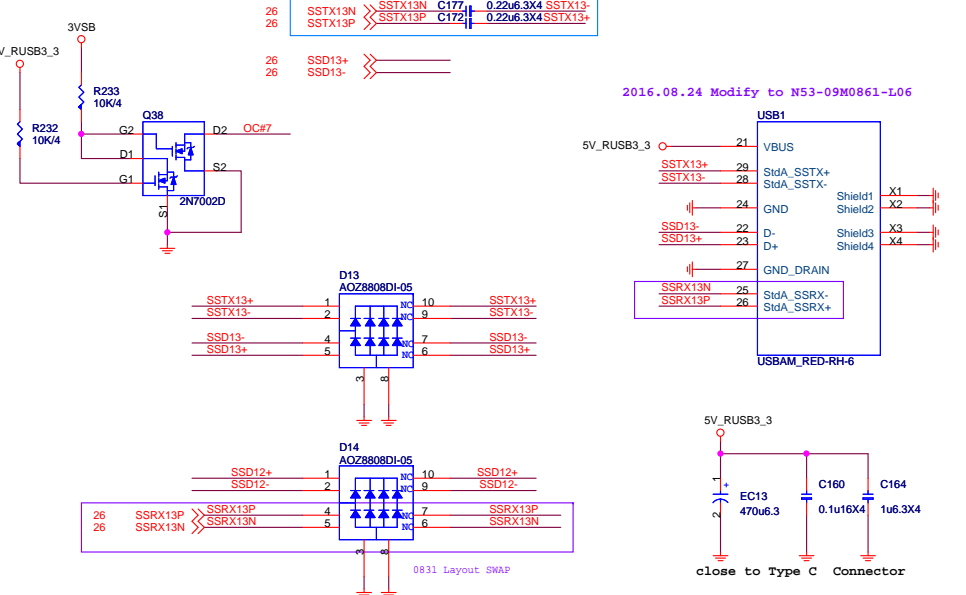
VBUS OC#



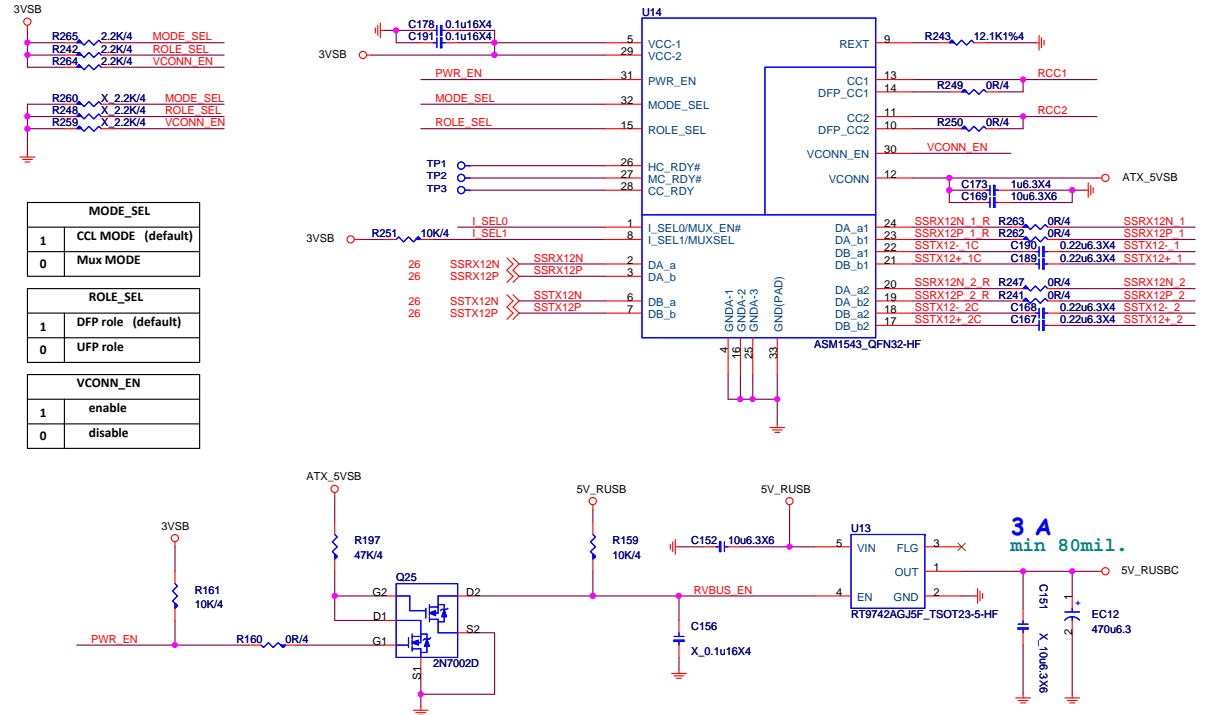
Current Mode



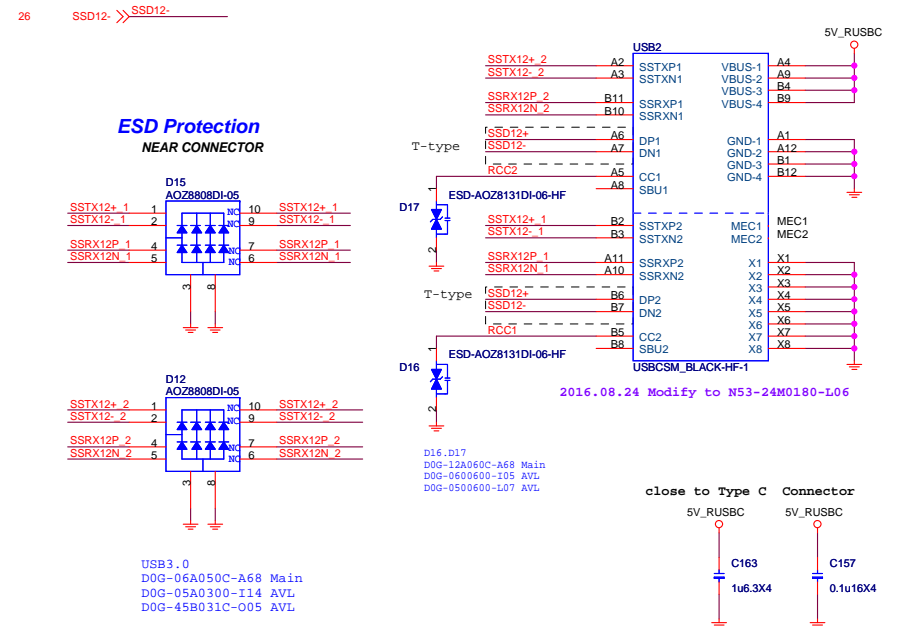
TYPE-A



USB Type-C MUX with Configuration Channel (CC)



TYPE-C



TO:NCT6779 GP72

H:SUPPORT S0/S3/S5
L:SUPPORT S0/S3

5VSDRV2, 5VSBDRV2 width 12mil,
do NOT route near the edge of a board.

ATX_5VSB

5V_SBDVRV_USB

C59
X_18n16

Q22
P-P06P03

5V_RUSB

Q20
NIKO/PK632BA

VCC5

6.7A+3A (TypeC)

5V_RUSB

F1
F-SPR-P260T-HF

2 1A

6V_RUSB2_1

PS_USB2.0

F3
F-SMD1206P350SLRT-G-HF

2 3A

6V_RUSB3_1

hdmi USB3.0

F4
F-SPR-P260T-HF

2 1.8A

6V_RUSB3_2

lan USB3.0

F2
F-SPR-P260T-HF

2 0.9A

6V_RUSB3_3

TypeA USB3.1

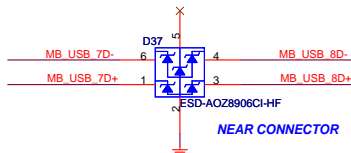
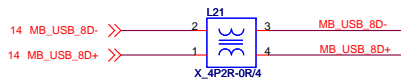
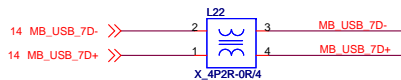
VR 1.5A*2

[illegible]

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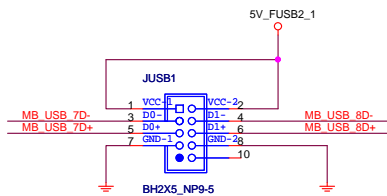
**MS-7A63**

Size Custom	Document Description USB POWER UP7501	Rev 10
Date: Tuesday, September 13, 2016		Sheet 28 of 69

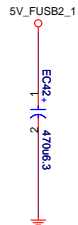
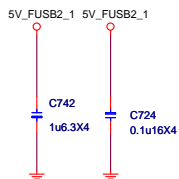


Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14

1.0A



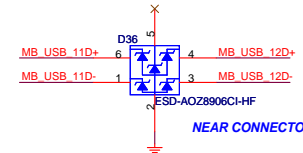
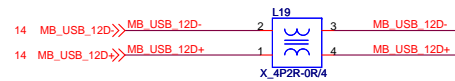
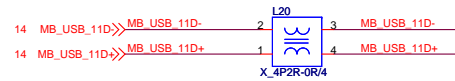
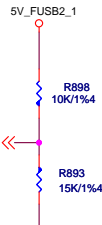
EMI Cap near Connector.



PORT7.8

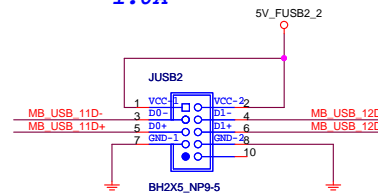
14

OC#3

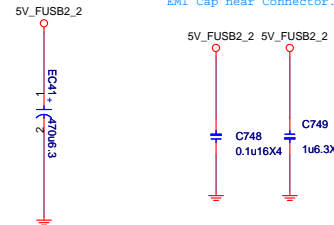


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AVL:D0G-45B0510-I14

1.0A



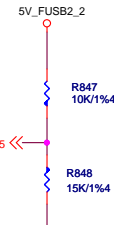
EMI Cap near Connector.



PORT11.12

14

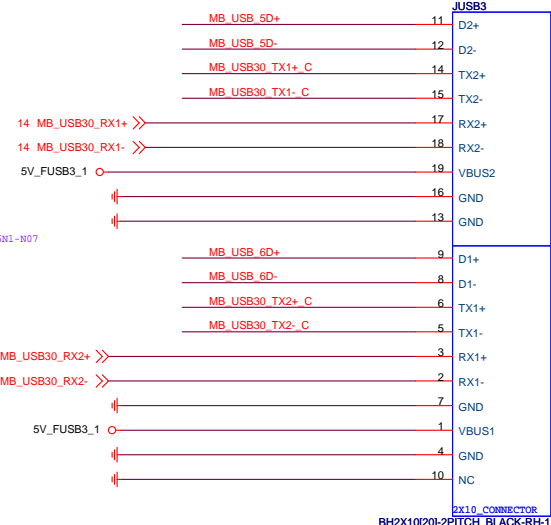
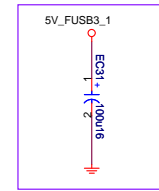
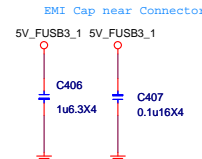
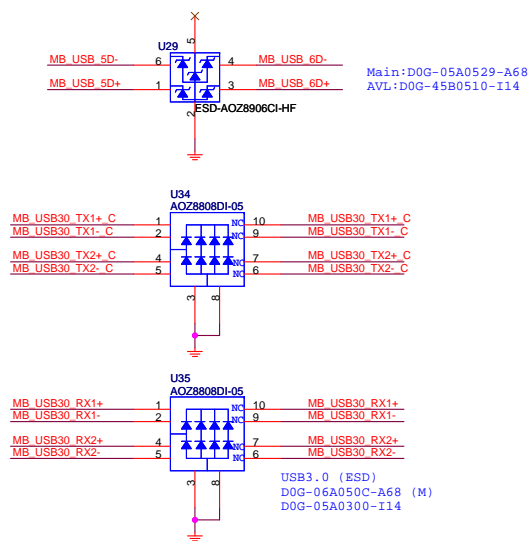
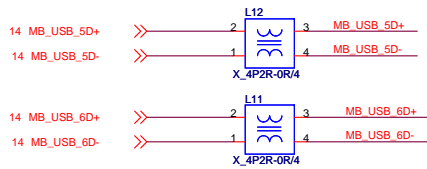
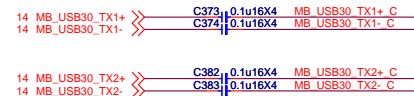
OC#5



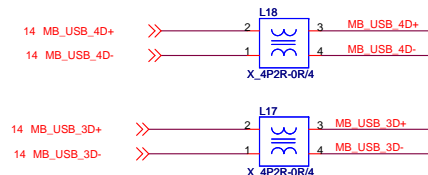
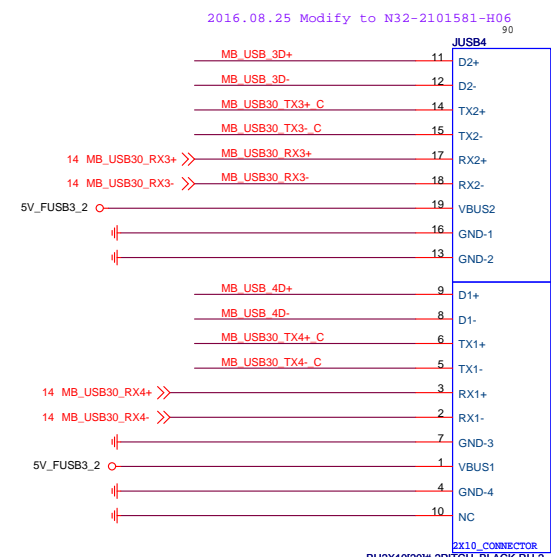
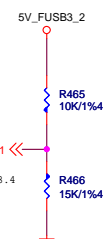
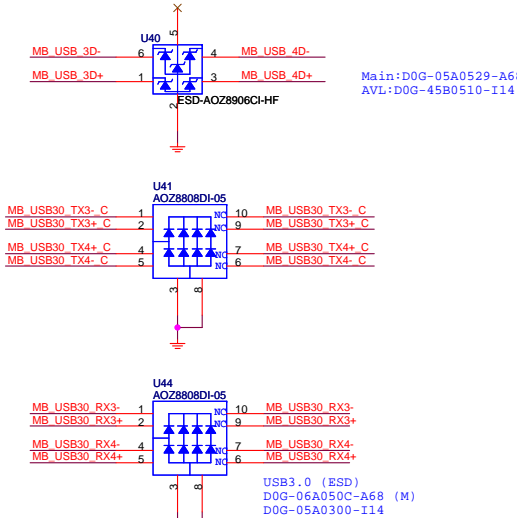
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Size	Document Description	Rev
Custom	Front USB20	10
Date:	Tuesday, September 13, 2016	Sheet 29 of 69

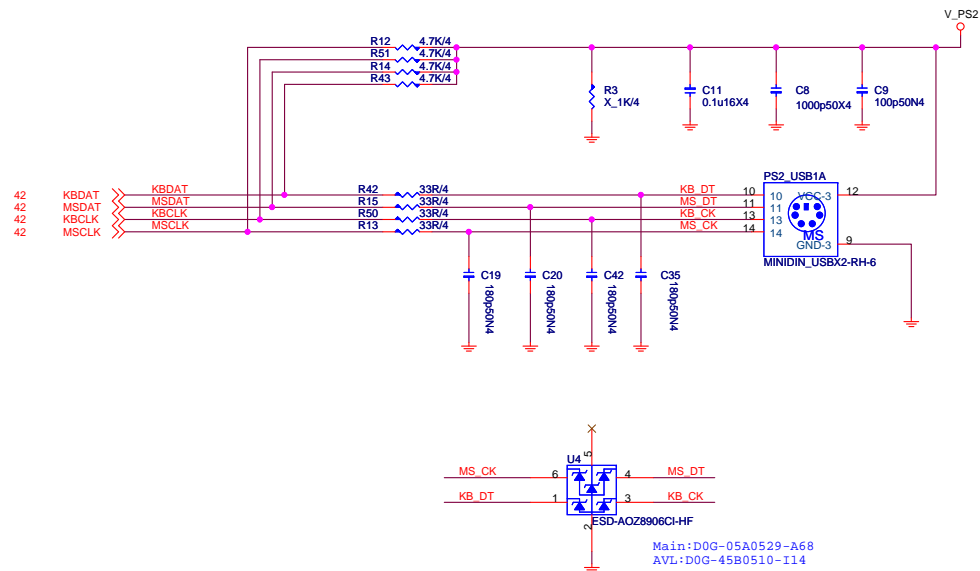


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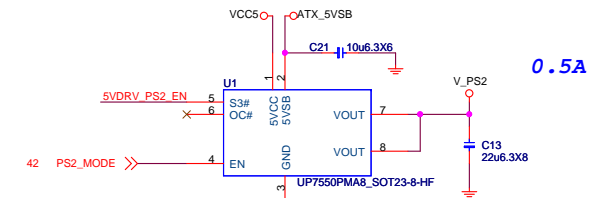


			
MICRO-STAR INT'L CO.,LTD			
MS-7A63			
Size	Document Description	Rev	
Custom	Front USB30	10	
Date:	Tuesday, September 13, 2016	Sheet	30 of 69

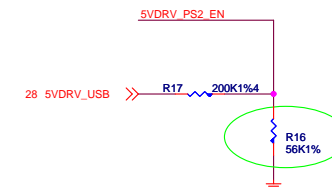
PS2 Connector



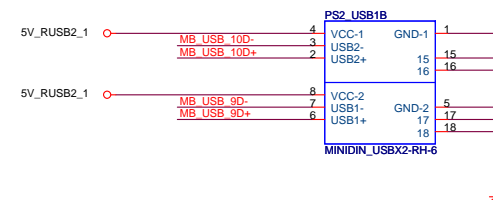
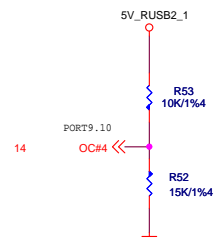
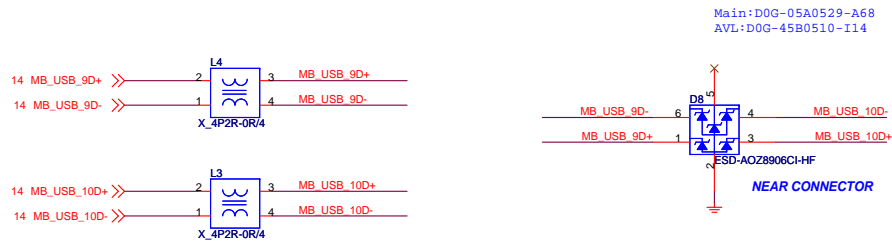
PS2 Power



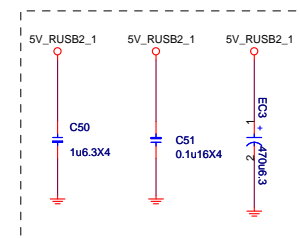
USB MODE



PS2 _USB



Close to Connector

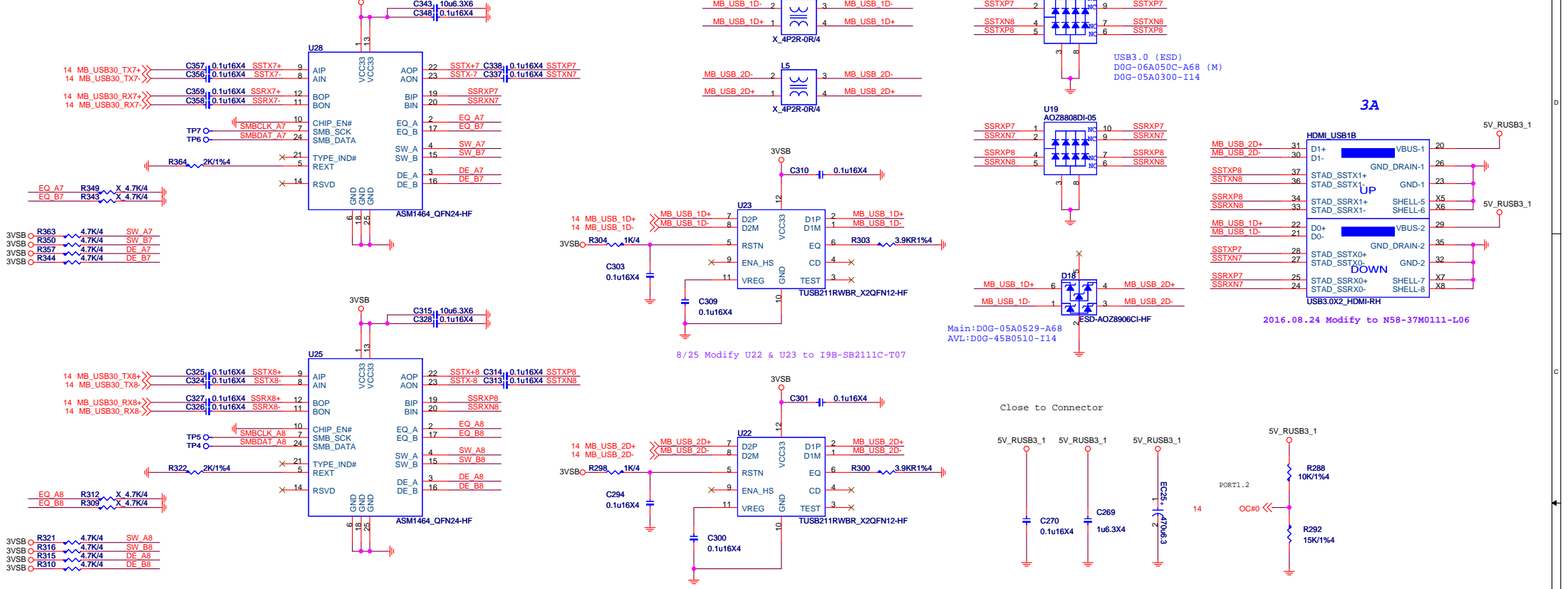


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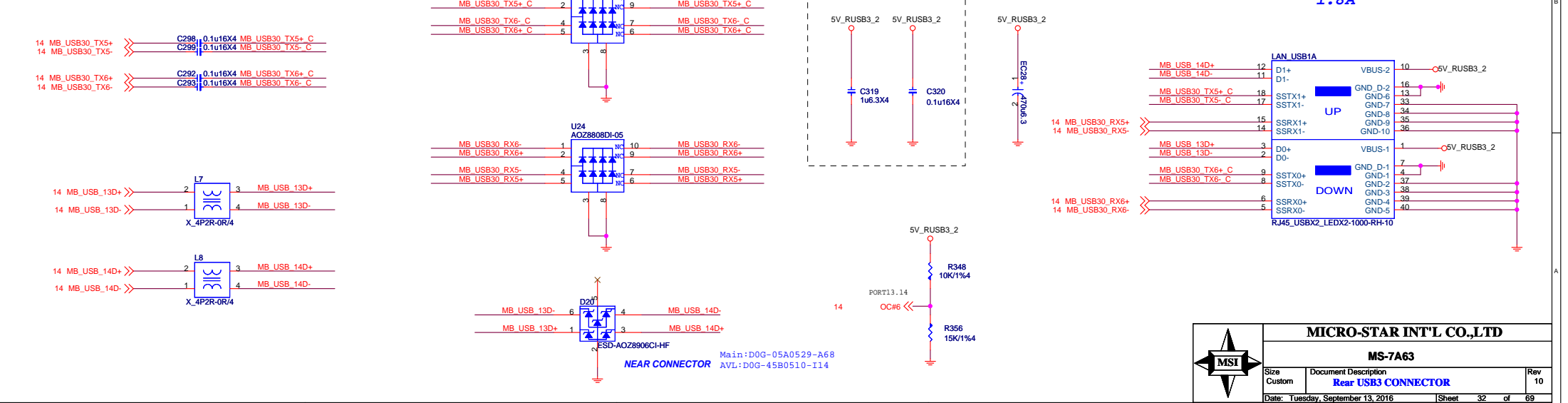
MS-7A63

Size Custom	Document Description Real USB2&PS2 CONNECTOR	Rev 10
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HDMI USB3.0

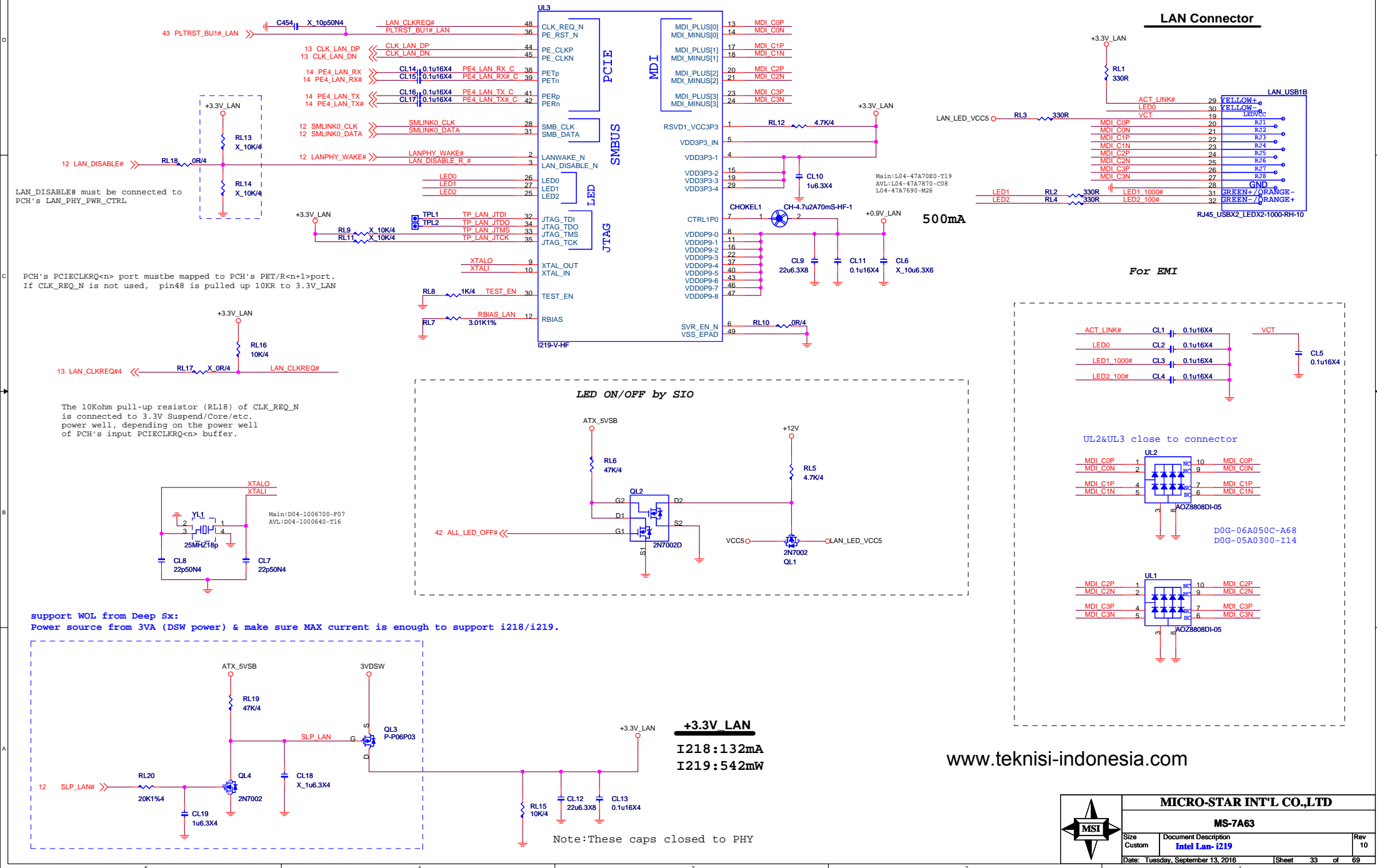


LAN USB3.0

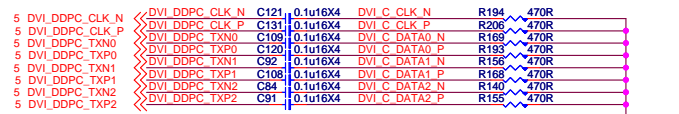


Intel Lan- i219

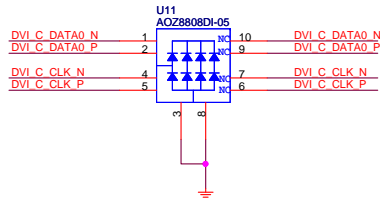
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8111G:B06-081116C-R09



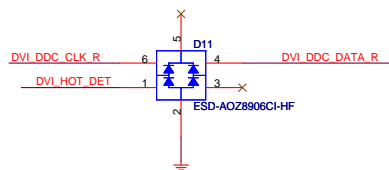
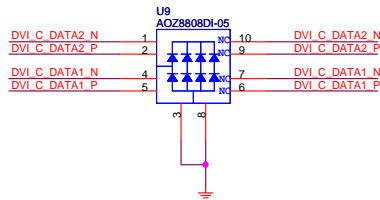
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



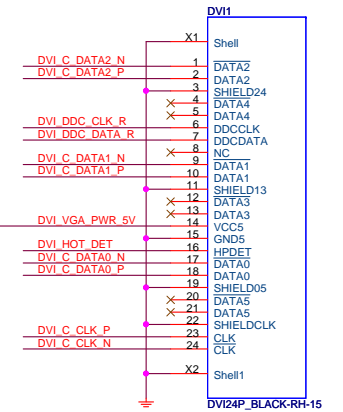
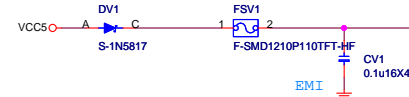
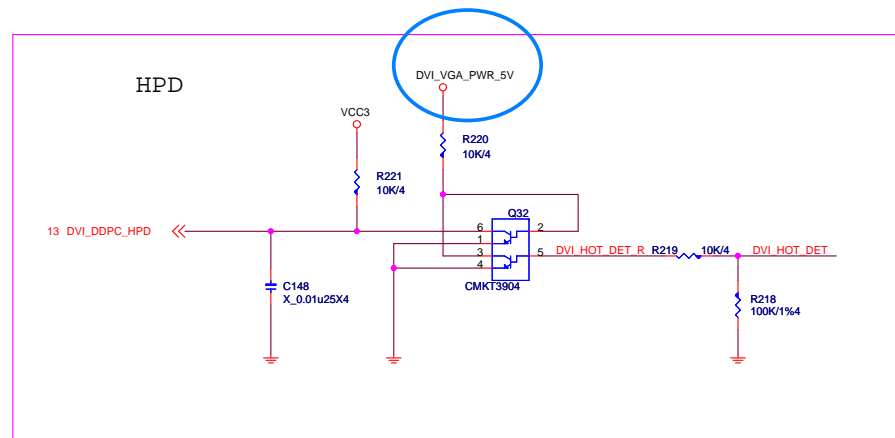
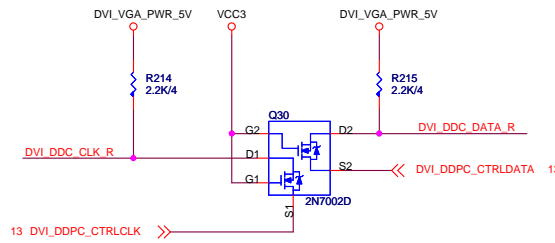
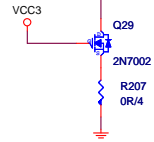
U26 AVL:D0G-05A050C-005
D0G-06A050C-A68



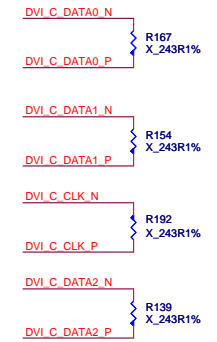
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D0G-06A050C-A68



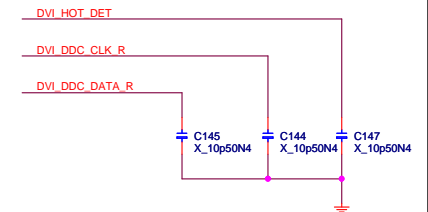
Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14



For EMI



EMI

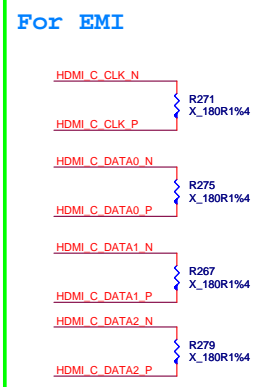
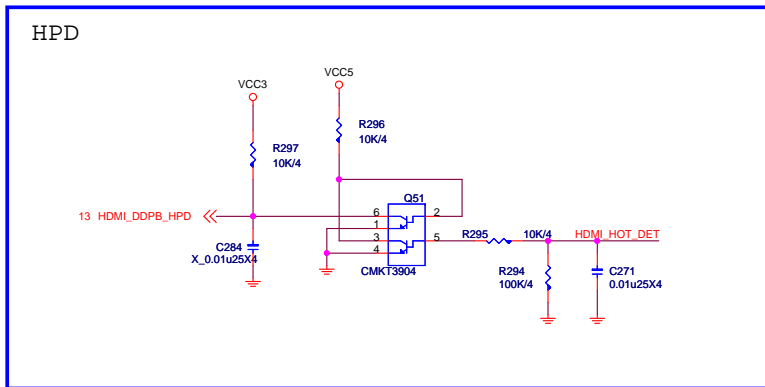
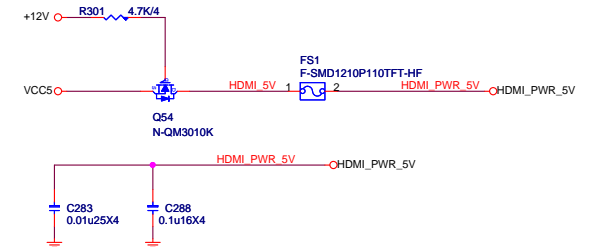
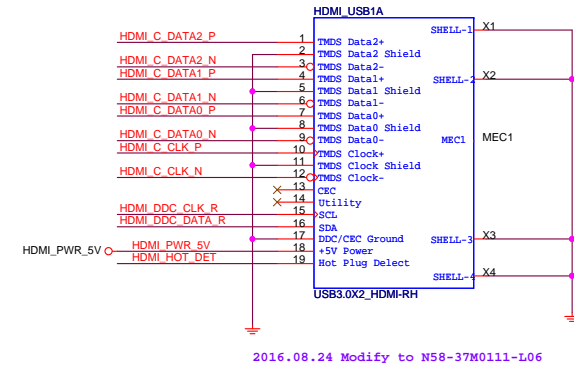
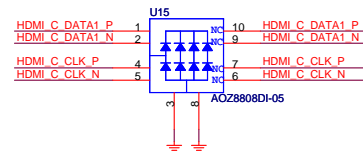
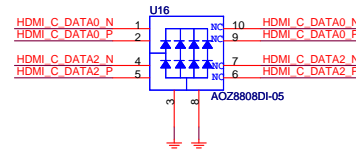
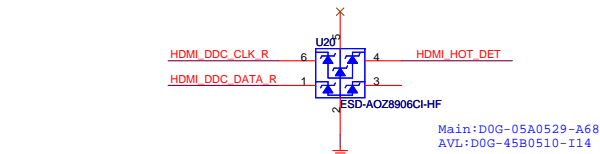
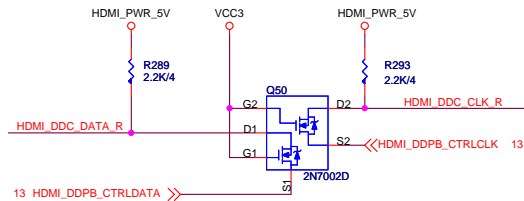
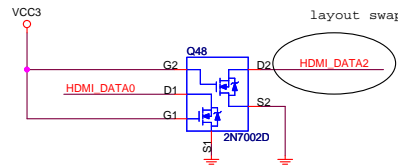
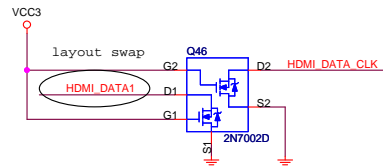
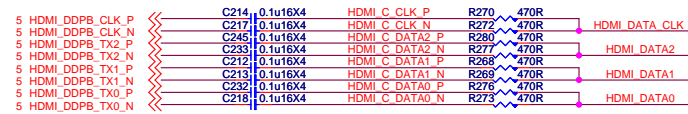


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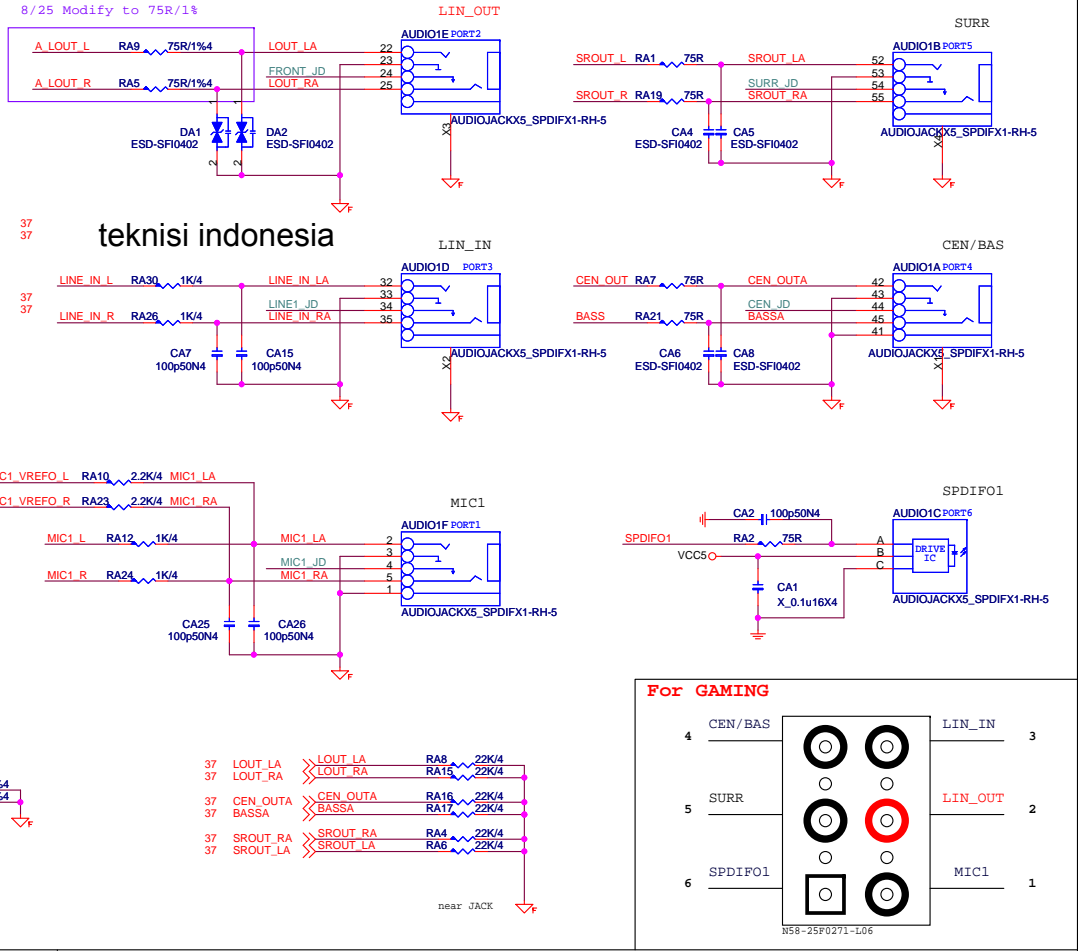
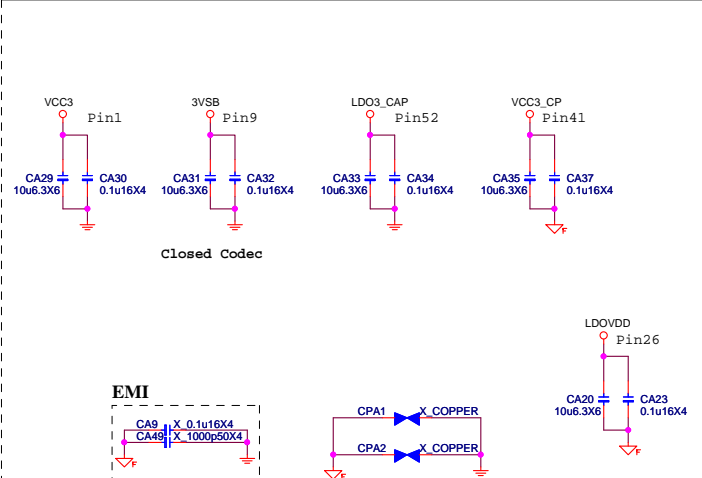
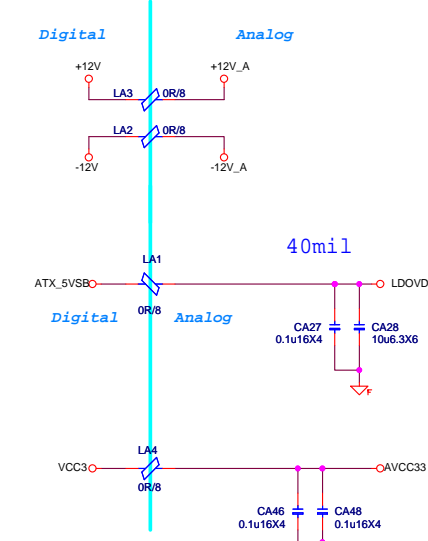
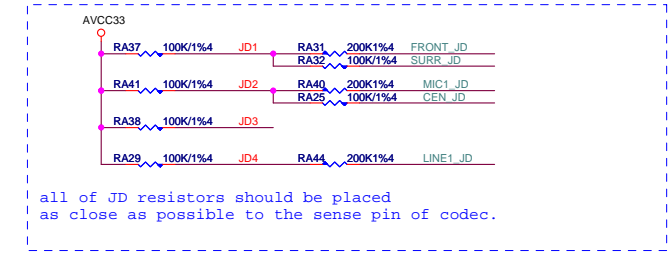
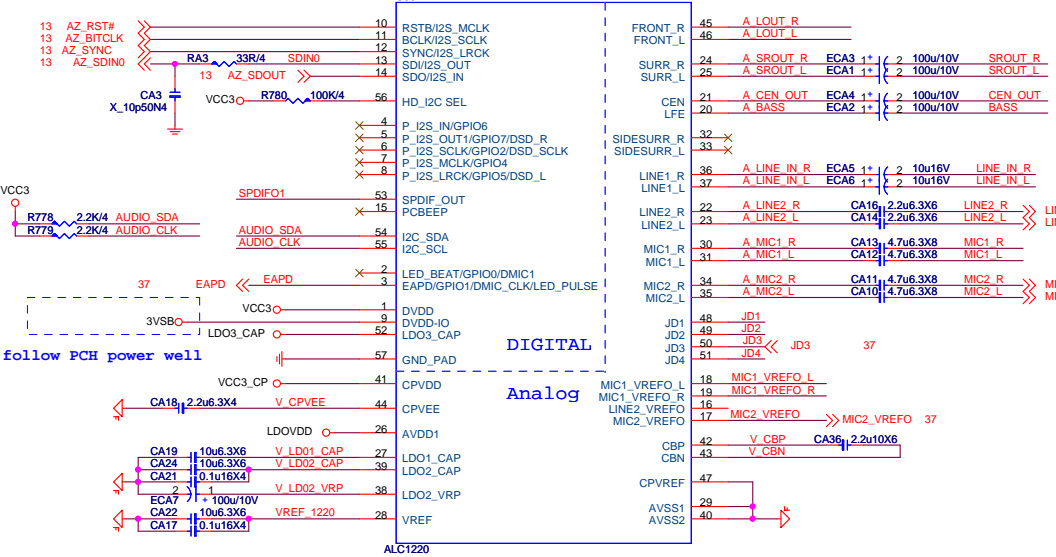
MS-7A63

Size	Document Description	Rev
Custom	DVI Connector	10
Date: Tuesday, September 13, 2016	Sheet 34 of 69	

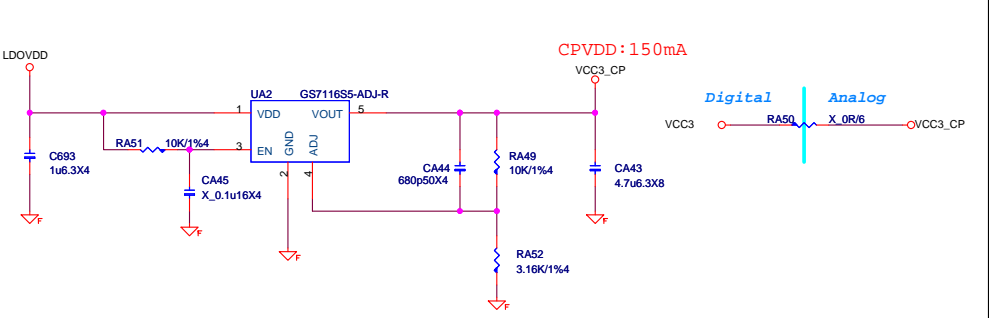
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



ALC1220



CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V

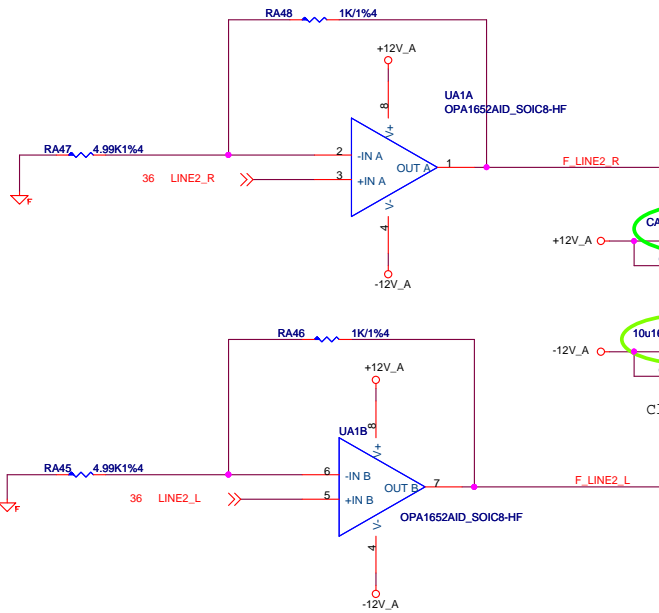


MICRO-STAR INT'L CO.,LTD

MS-7A63

Size Custom Document Description **AUDIO ACL1220-1** Rev 10

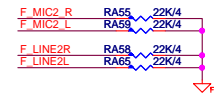
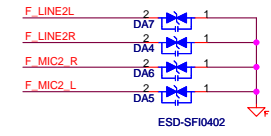
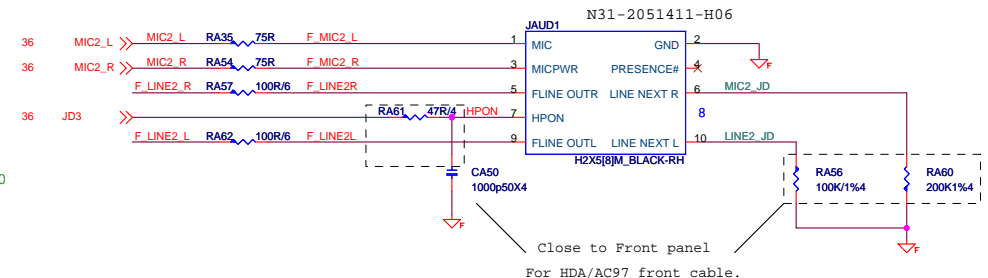
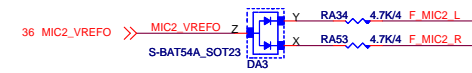
Date: Tuesday, September 13, 2016 Sheet 36 of 69



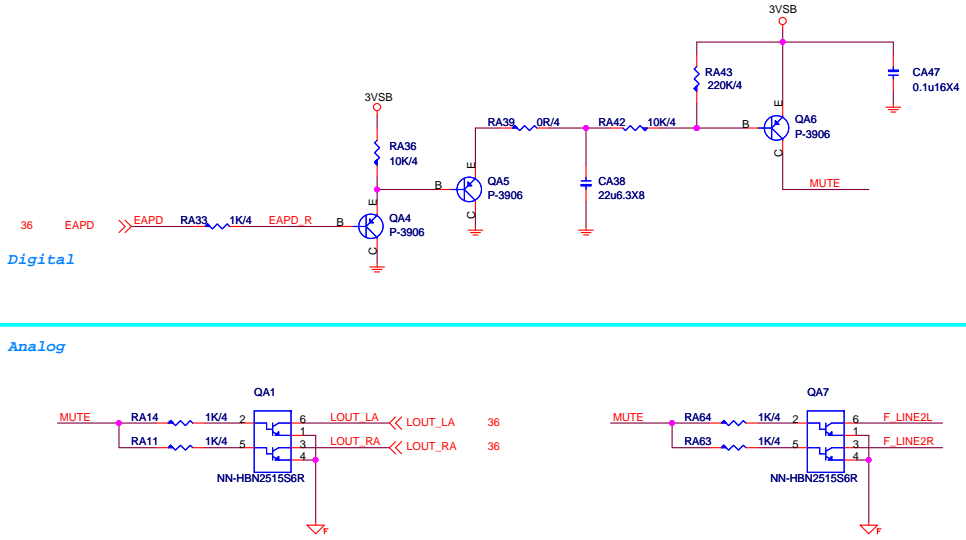
OC : C11-1067514-T04
GAMING: C91-1001631-N10

Close to U3

Close to Jack
ESD protect
D0G-2710510-I05
D0G-2950500-S10



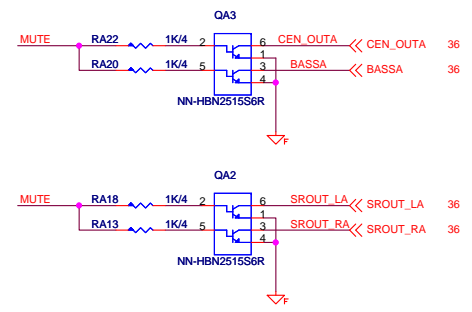
Rear Line OUT De-POP circuit (De-pop circuit for Rear Line out & Front Headphone out)



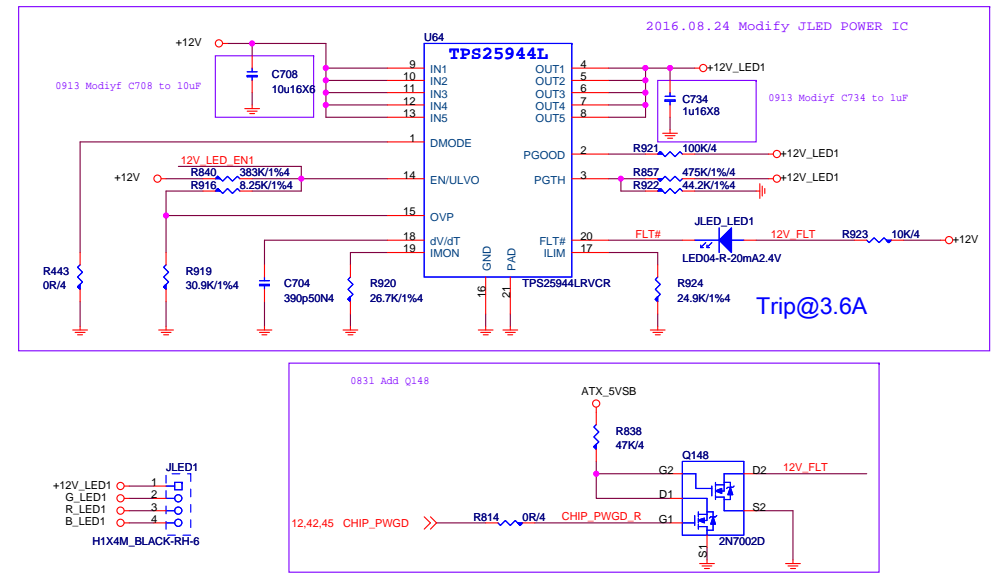
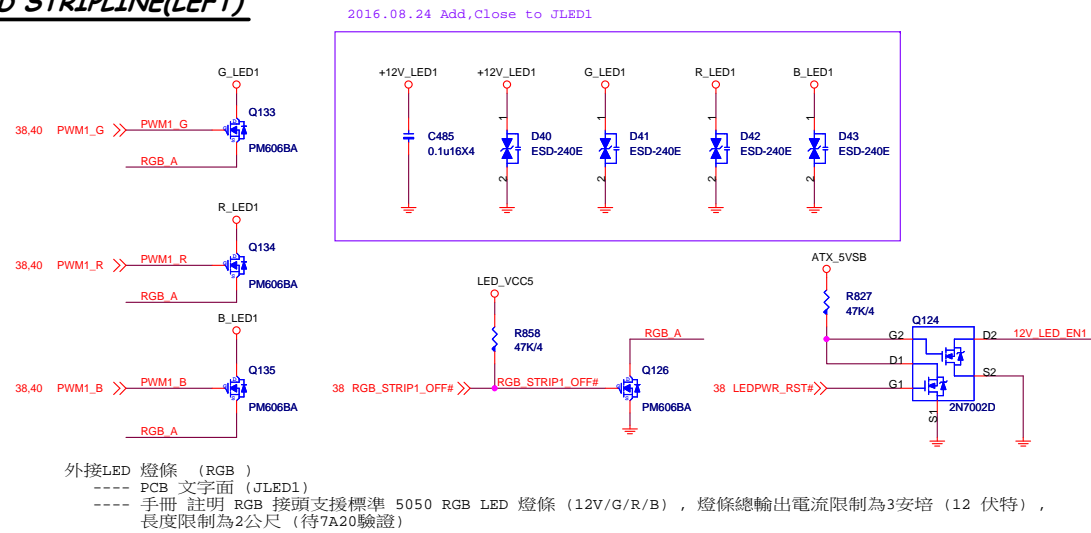
Digital

Analog

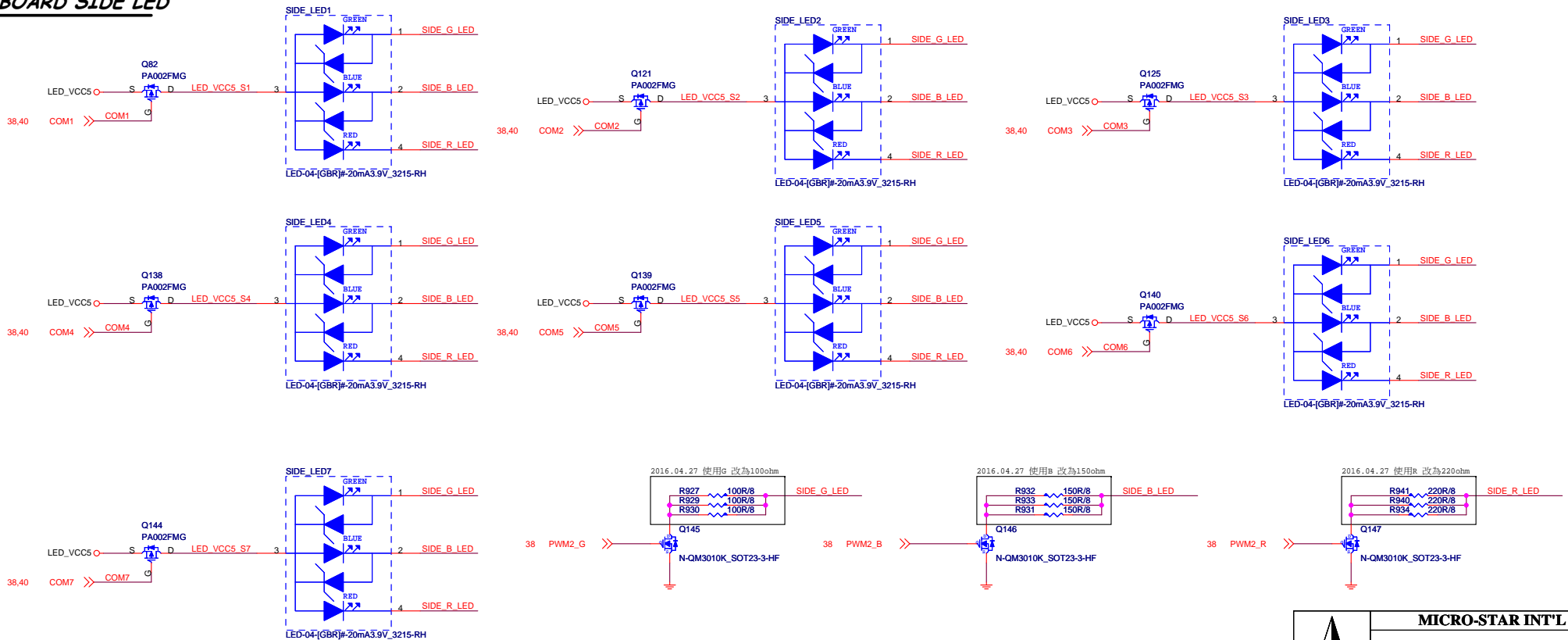
(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA4,CA5, CA6, CA8,to TVS)



LED STRIPLINE(LEFT)

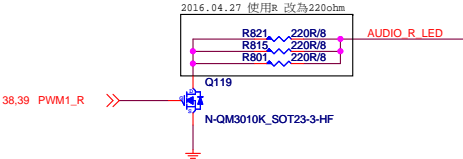
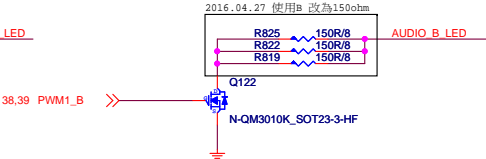
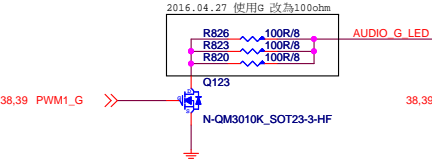
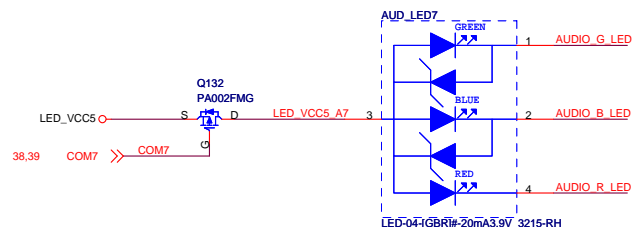
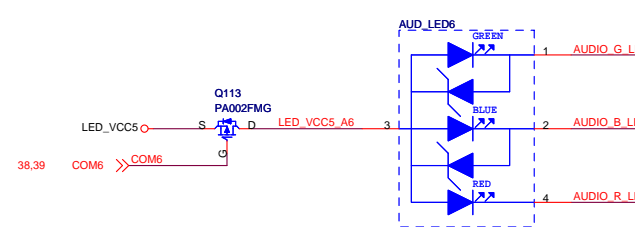
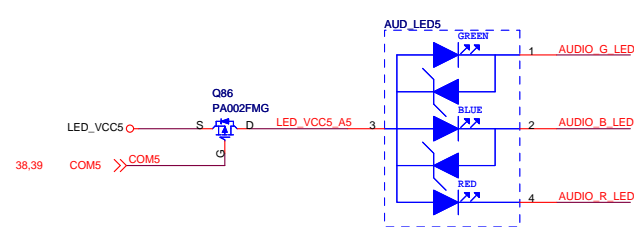
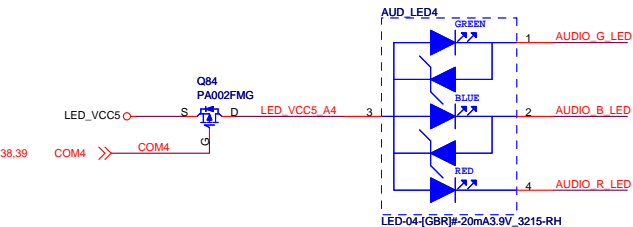
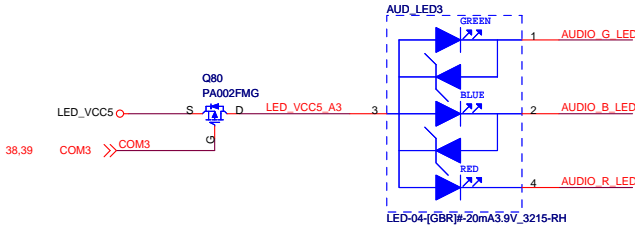
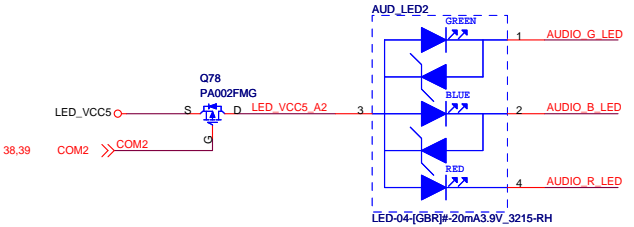
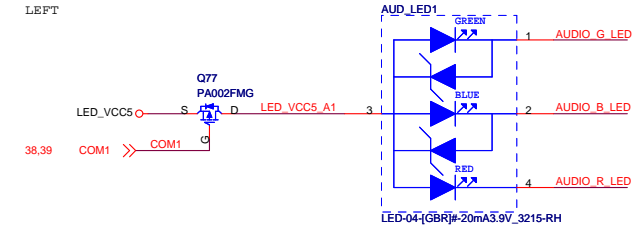


BOARD SIDE LED



AUDIO_MOAT LED

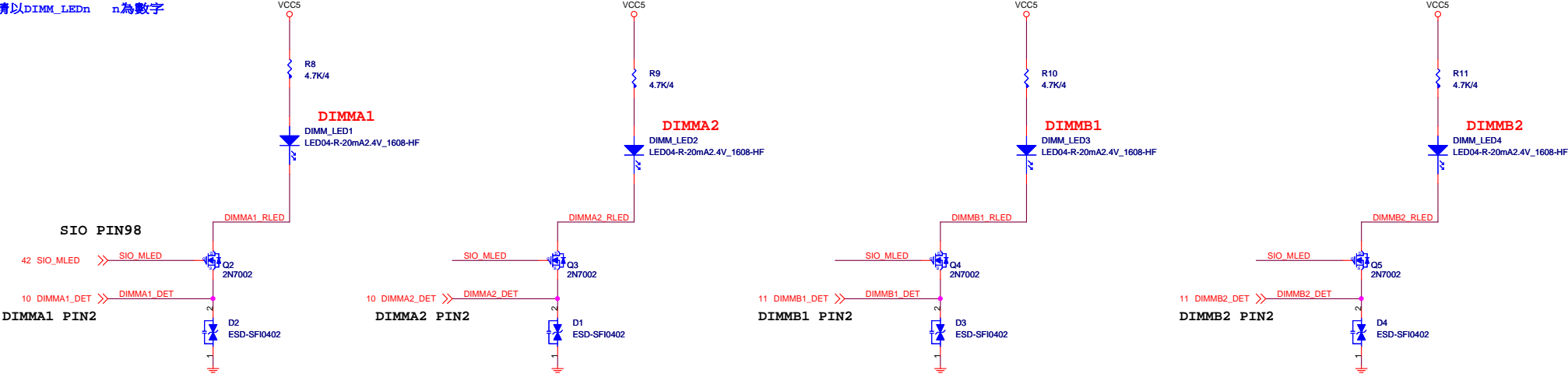
LEFT



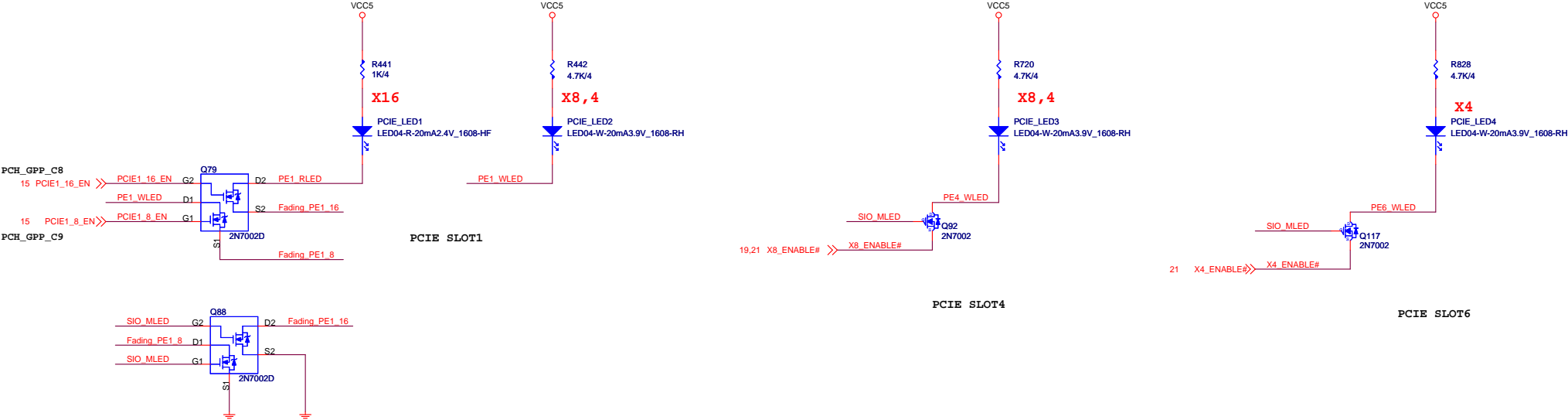
DIMM_SLOT

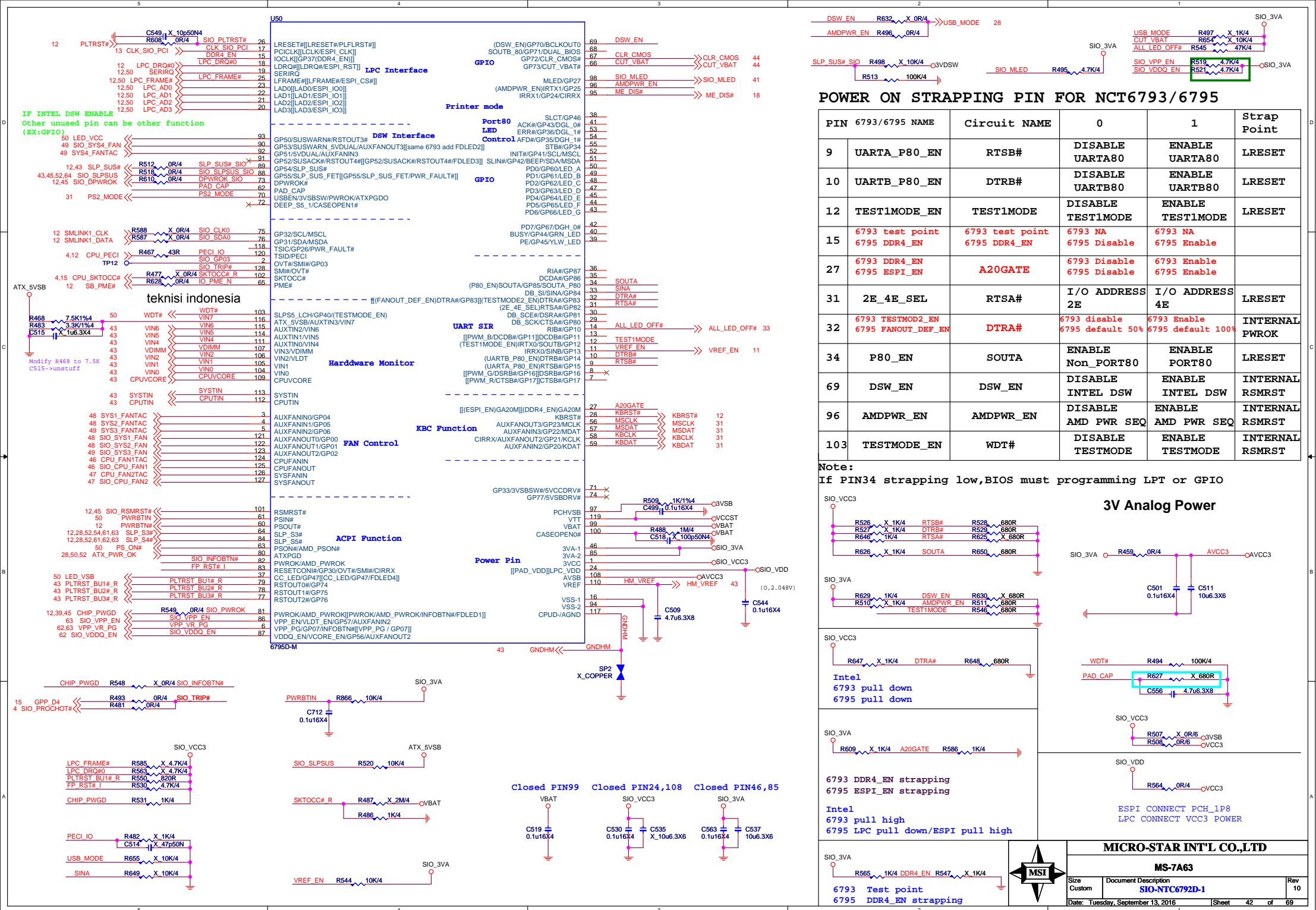
紅：D0C-040S500-E07

LED 命名請以DIMM_LEDn n為數字



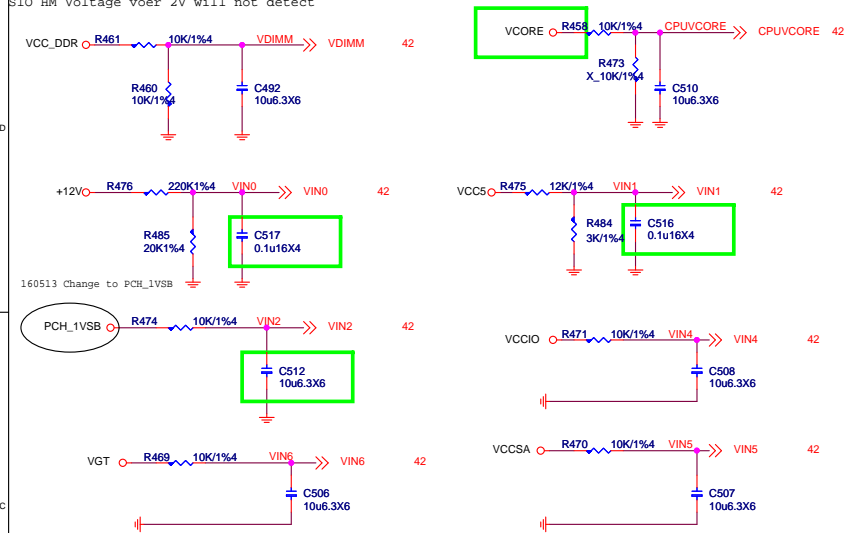
PCIE SLOT LED



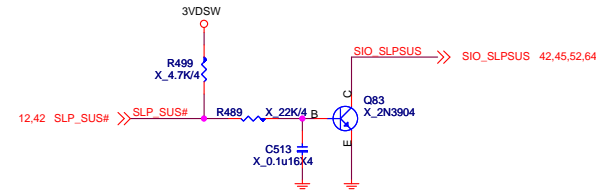


HW Monitor - Voltage

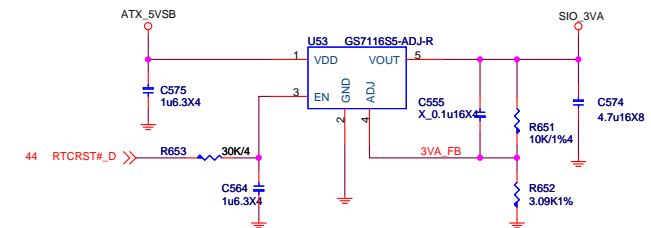
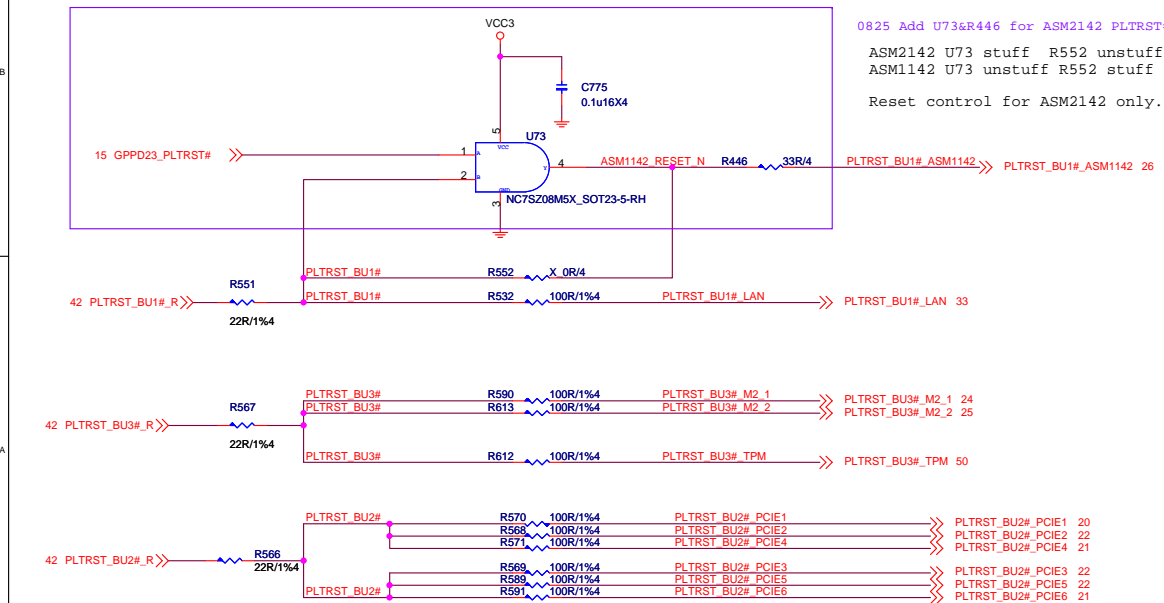
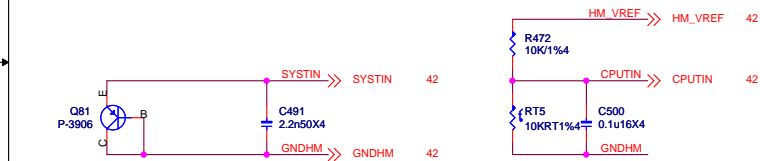
SIO HM Voltage voer 2V will not detect



SLP_SUS Co-lay circuit

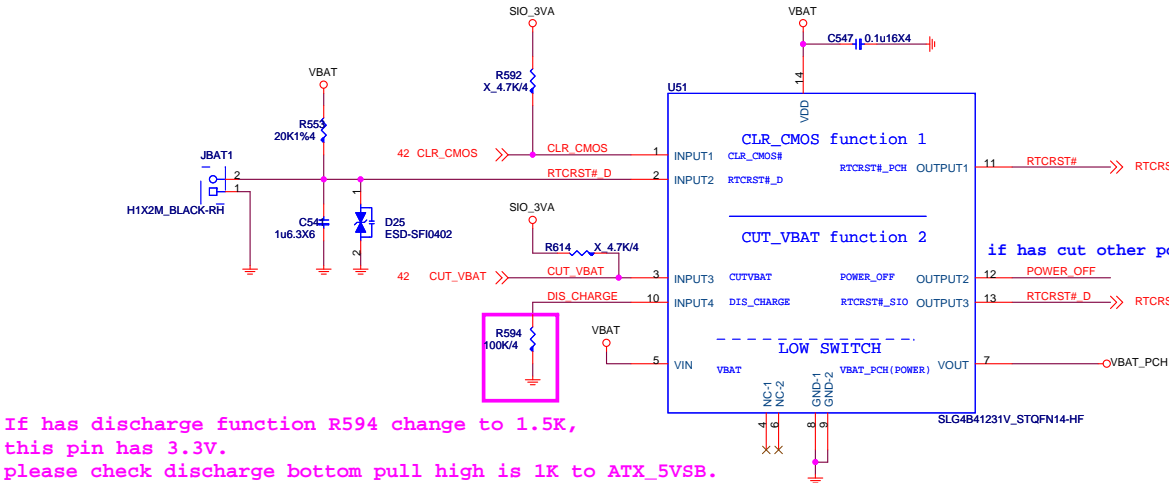


Thermal Monitor

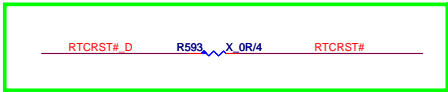


CLR_CMOS

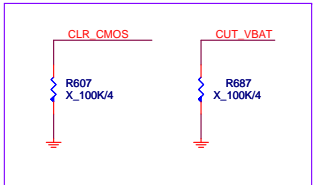
VBAT



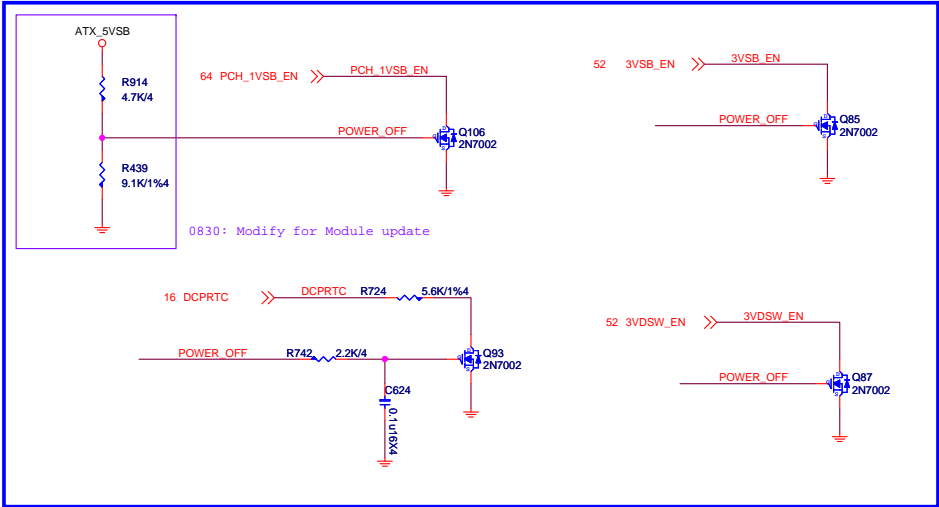
If has discharge function R594 change to 1.5K, this pin has 3.3V. please check discharge bottom pull high is 1K to ATX_5VSB.



Co-Lay NOT USE U12 , R139 STUFF
If STUFF R139 Please Check RTCRST# Double Pull High



0830: Add R607.R687 for Module update



Function 2					
IN		OUT			
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT	
0	0	0	1	1	
1	0	1	1	0 (discharge)	
0	1	1	0	0 (discharge)	
1	1	1	0	0 (discharge)	

Default

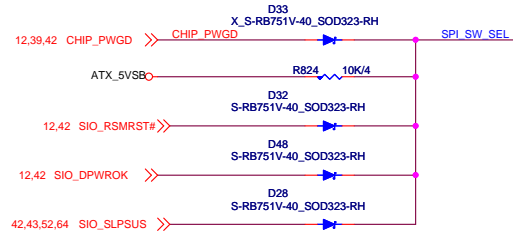
Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

Module Stuff CHIP_PWGD,
But PCH_PWROK may ramp up before CHIP_PWGD.

0825 Add D48, unstuff D33

For TL624 1.1

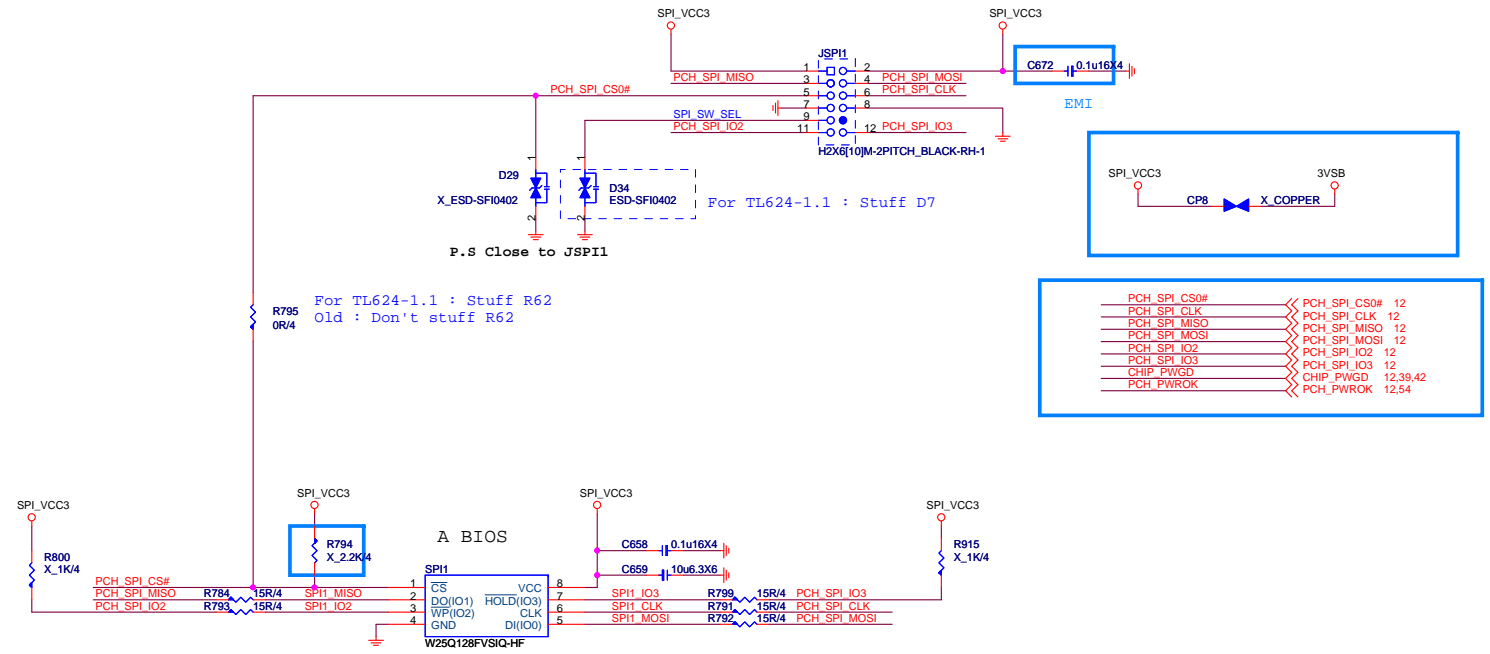


For TL624-1.1

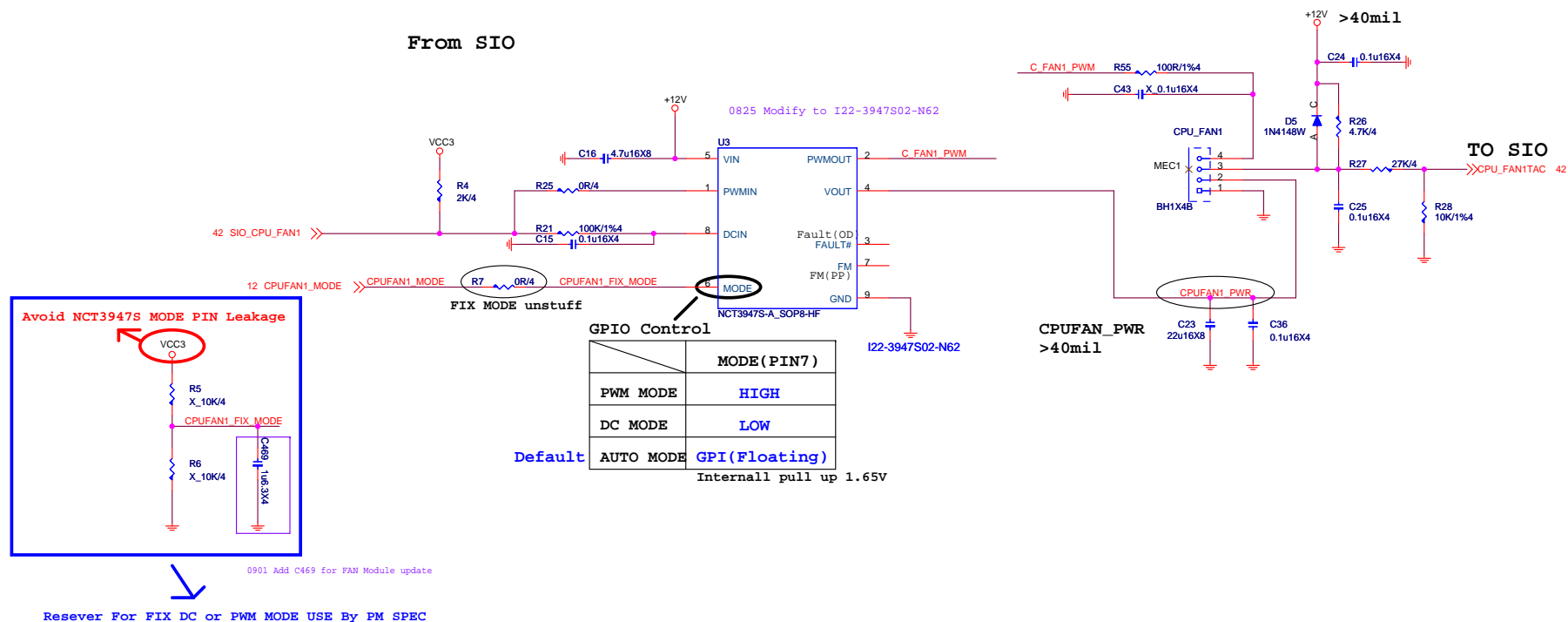
SKYLAKE : Stuff D10/D17/R353

B85/H87 : Stuff D8/D9/R353

Others : Stuff R272



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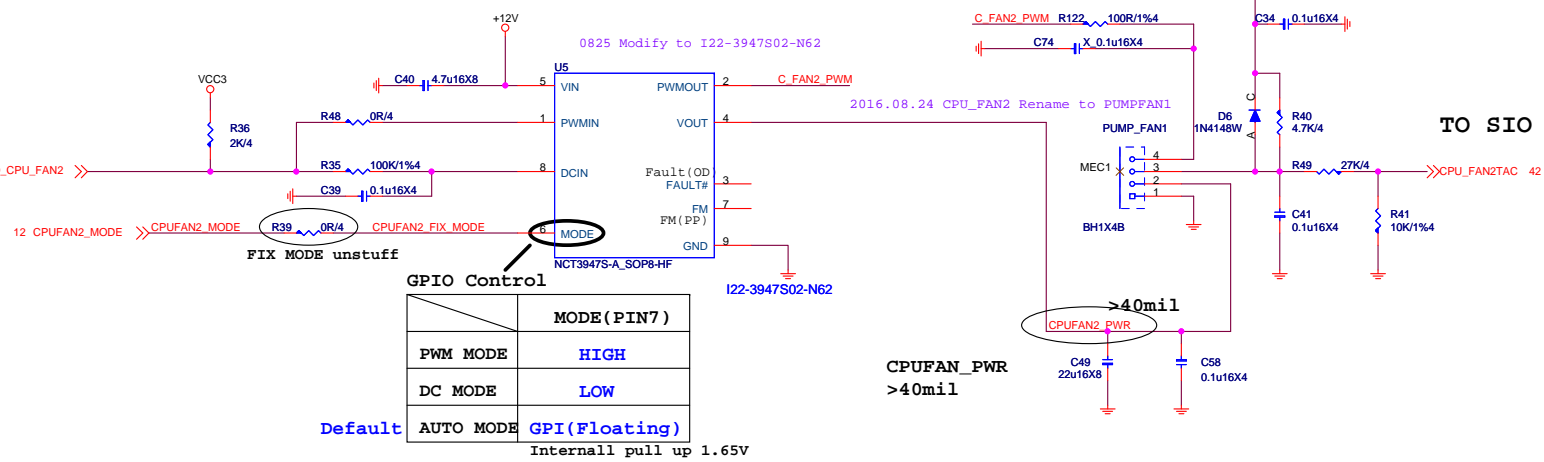
- 1.MODE : USE MODE PIN change FAN MODE(PWM or DC FAN)
- 2.FAULT : USE FAULT PIN Triger OVT/OCV Protection,LOW Atcive (Reserve NEW IC)
- 3.FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)



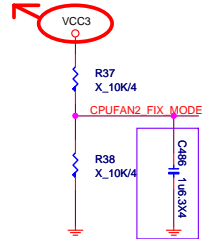
MICRO-STAR INT'L CO.,LTD		
MS-7A63		
Size Custom	Document Description CPU FANI	Rev 10
Date: Tuesday, September 13, 2016	Sheet 46 of 69	

TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

From SIO



Avoid NCT3947S MODE PIN Leakage

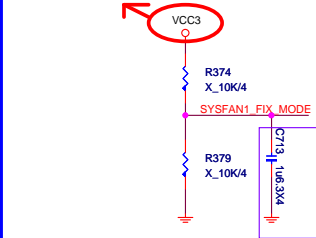


- 1.MODE : USE MODE PIN change FAN MODE(PWM or DC FAN)
- 2.FAULT : USE FAULT PIN Triger OVT/OC Protection,LOW Atcive (Reserve NEW IC)
- 3.FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)

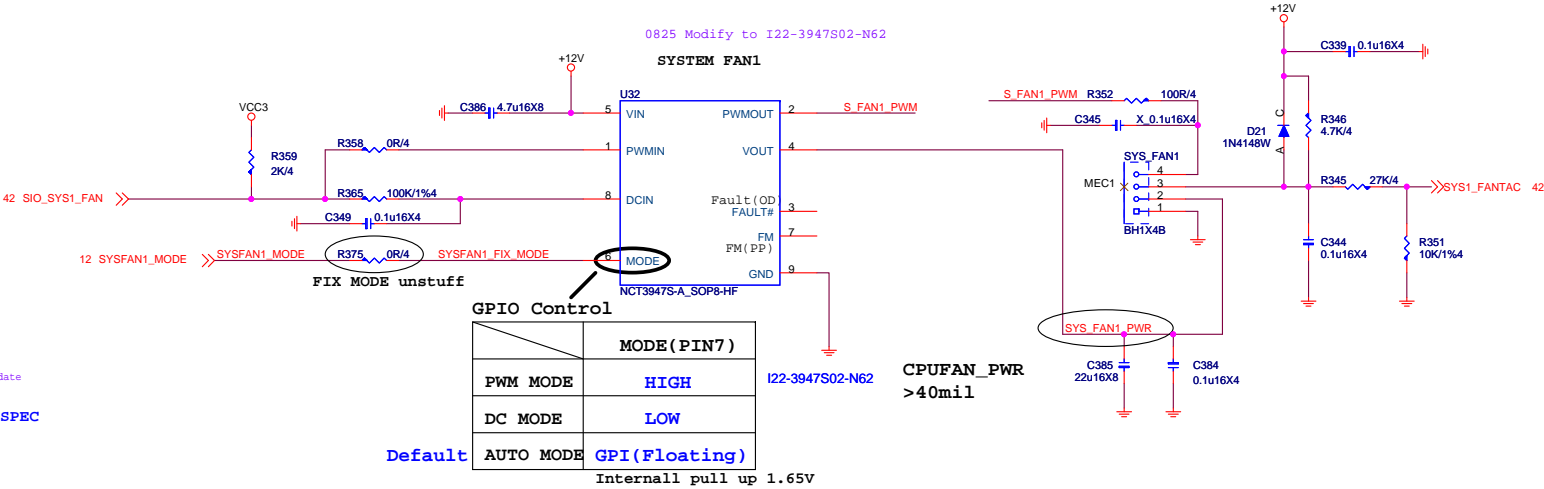


TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

Avoid NCT3947S MODE PIN Leakage

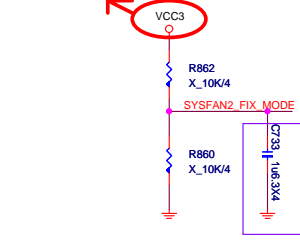


Resever For FIX DC or PWM MODE USE By PM SPEC

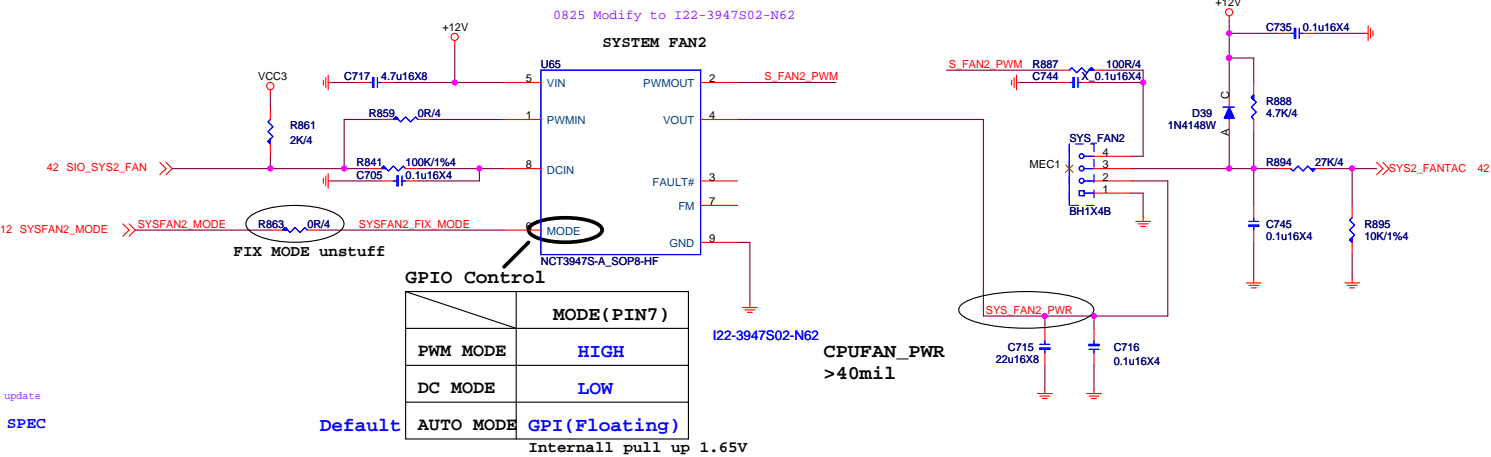


TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

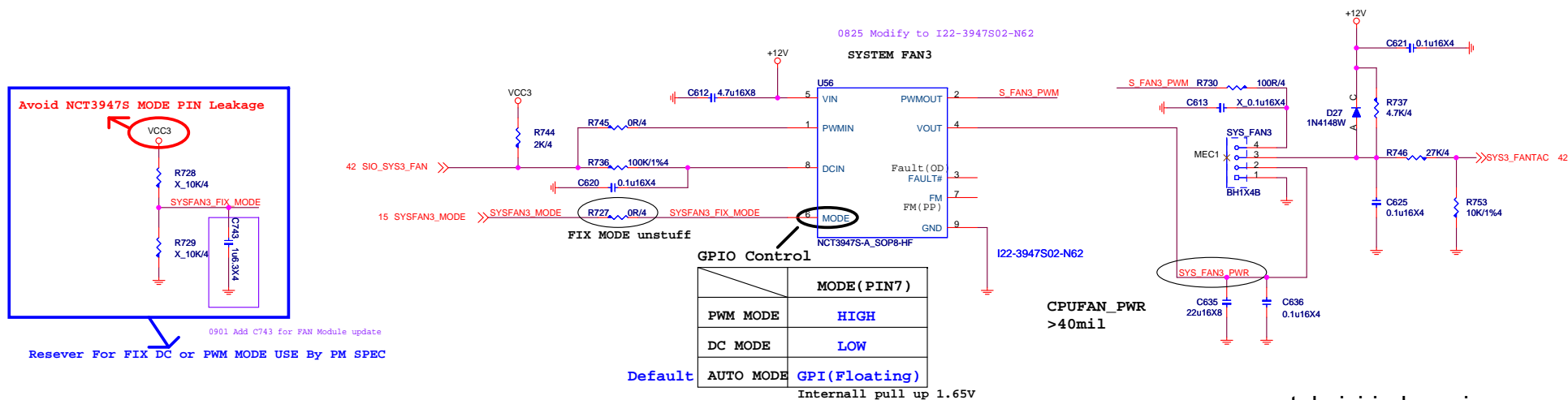
Avoid NCT3947S MODE PIN Leakage



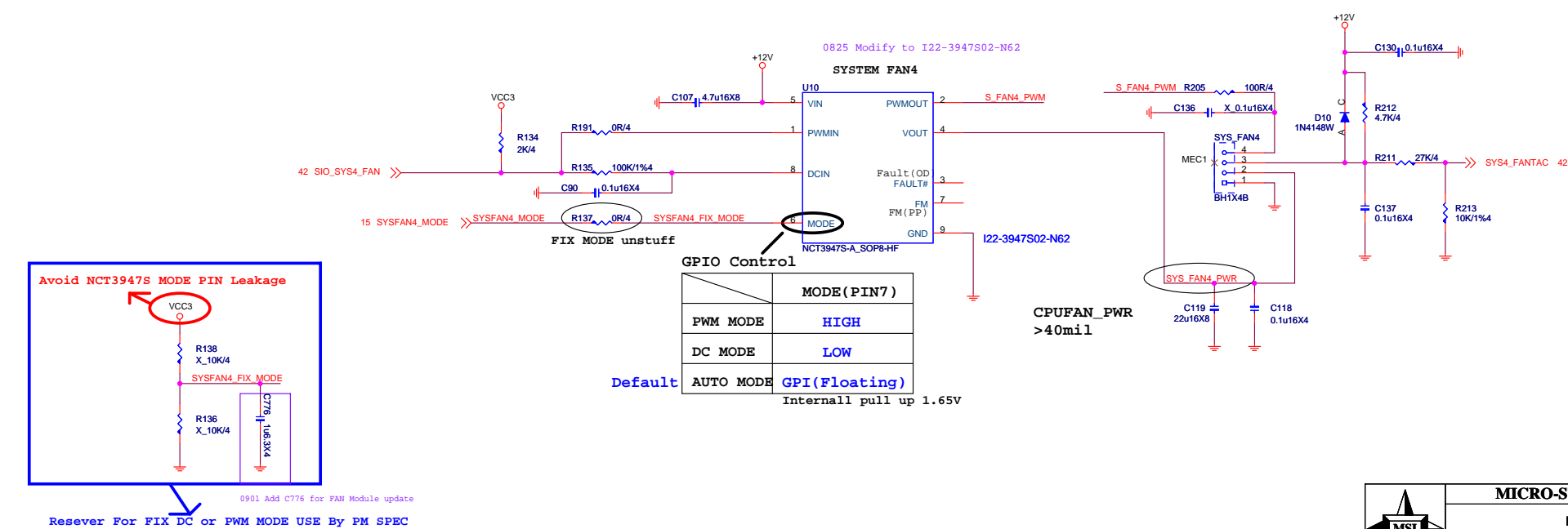
Resever For FIX DC or PWM MODE USE By PM SPEC



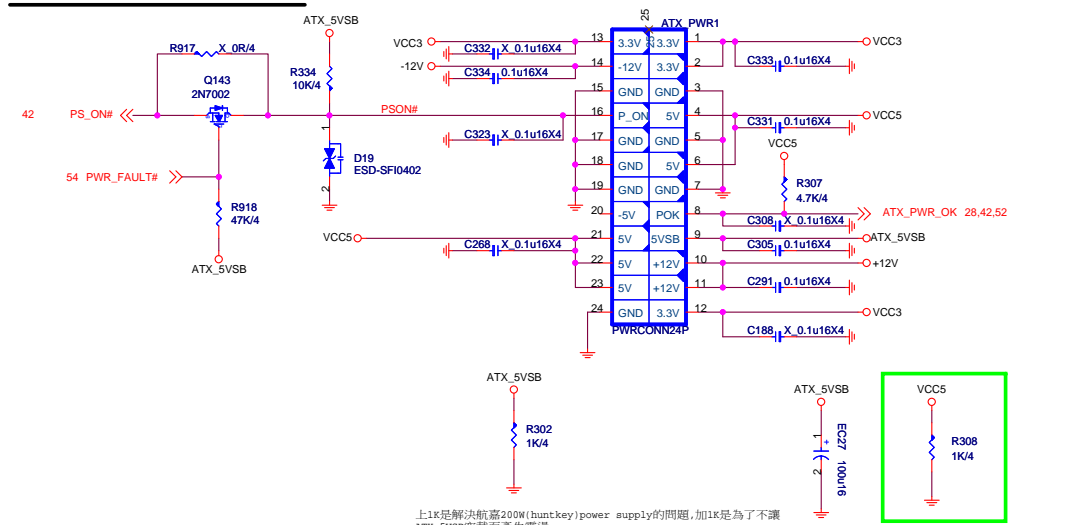
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



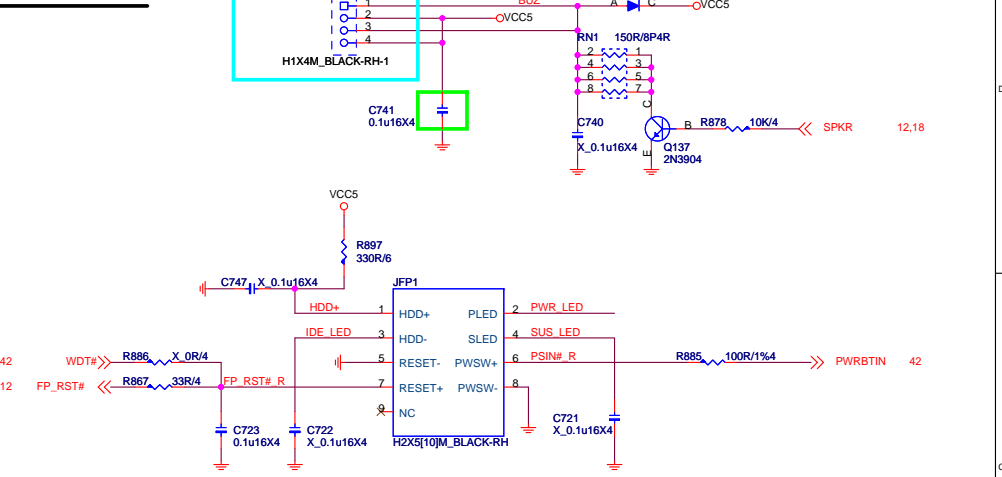
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



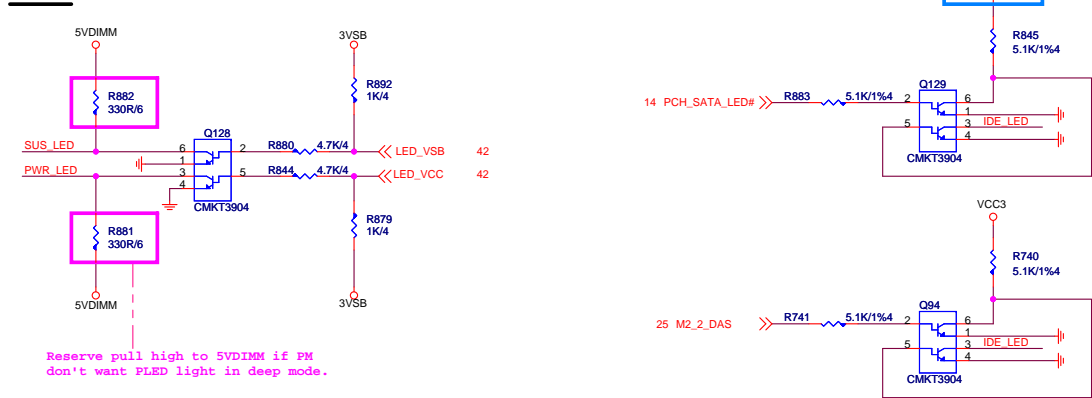
ATX POWER CONNECTOR



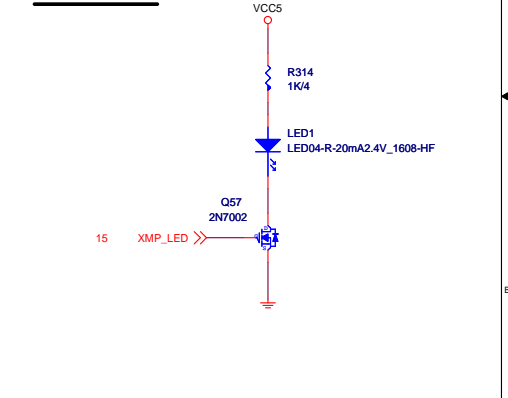
Front Panel



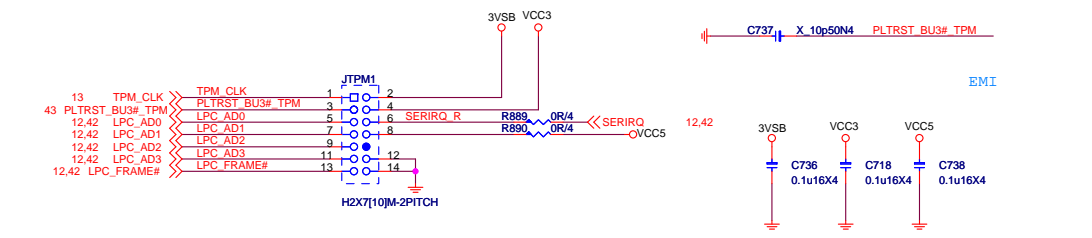
LED



XMP LED

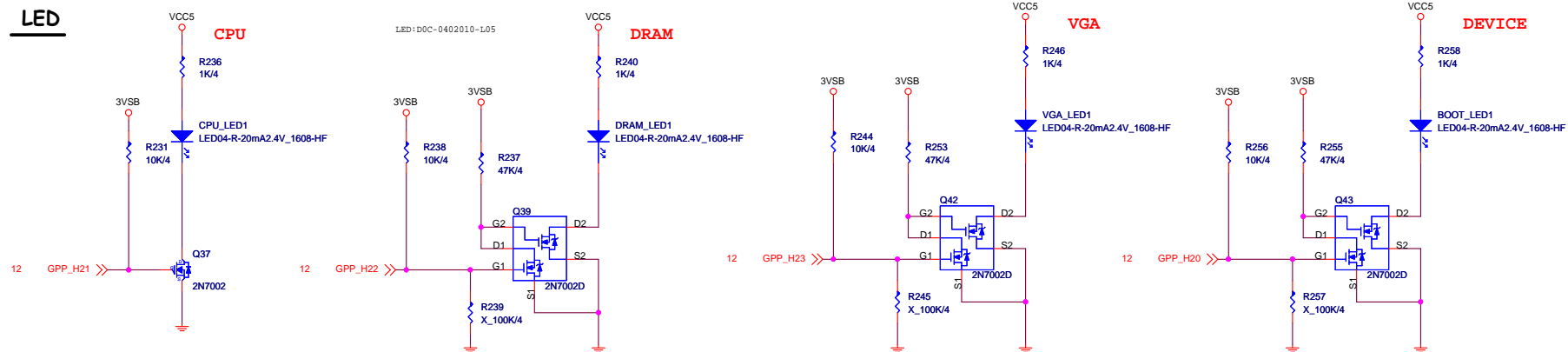


TPM Confirm ESPI TPM card and TPM card pin difine (Not ready)



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LED

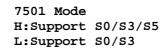


開機斷電狀態下，4個LED先維持default全暗，開機通電後：

1. 首先進行CPU check CPU LED 亮，check PASS後則CPU LED減掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED減掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED減掉。
4. 因此最後正常順利開機後，三個LED燈都是減掉的。
(系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作)

LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

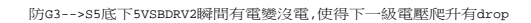
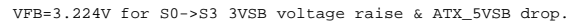
5.45A



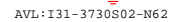
5VDUAL is power source of 1P0SB

[illegible]

4.04A



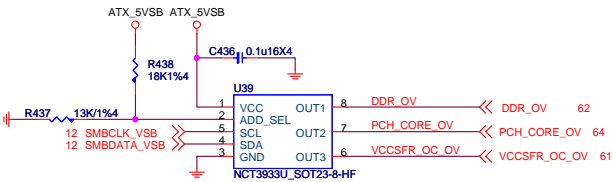
0.422A



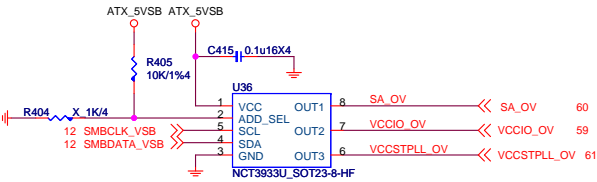
3VDSW_EN >> 3VDSW_EN 44

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



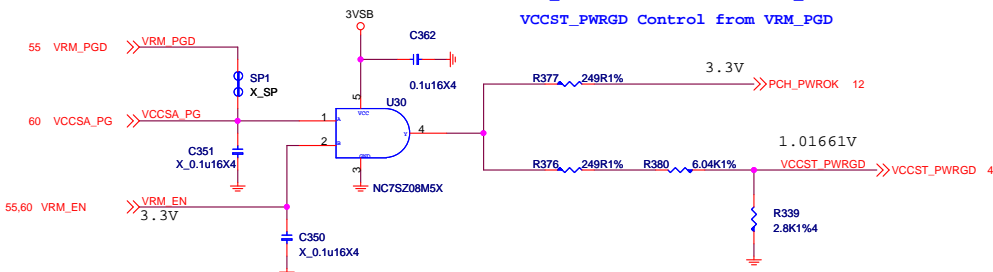
0x20:RH=10K,RL=OPEN



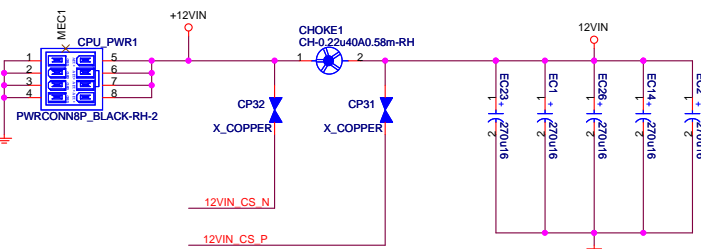
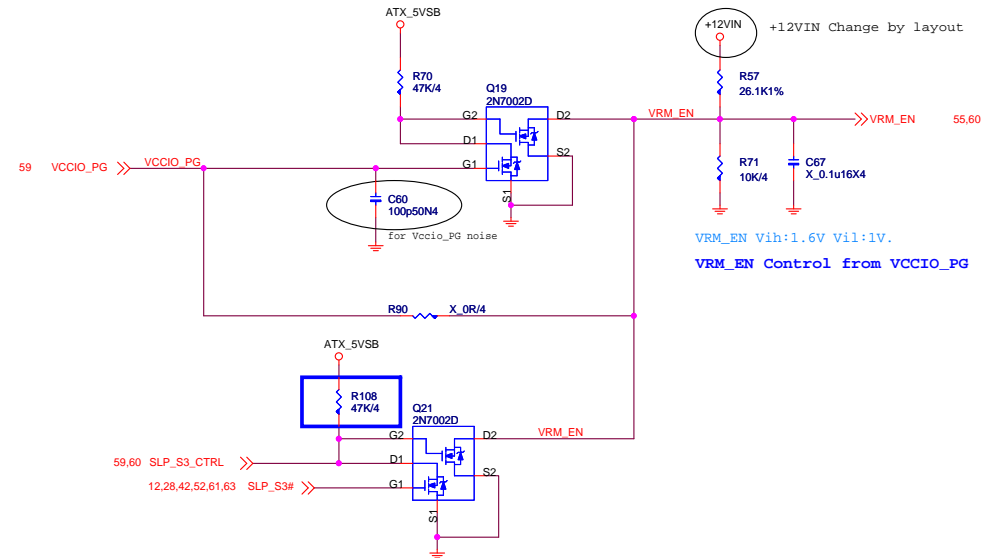
ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

VCCSA&Vcore use same PWM IC, pull up VCC3
VCCSA&Vcore use different PWM IC,pull up VCCSA
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.

PCH_PWROK Control from VCCIO_PG&VCCSA
VCCST_PWRGD Control from VRM_PG

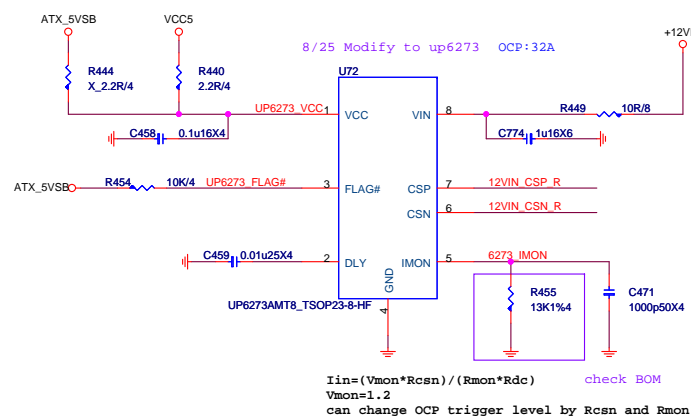
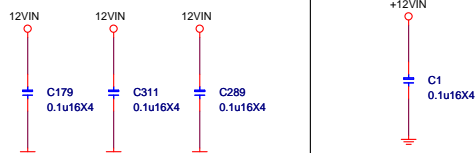


VRM_EN Control from VCCIO_PG

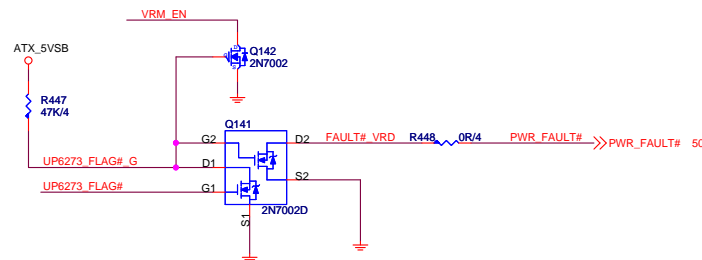
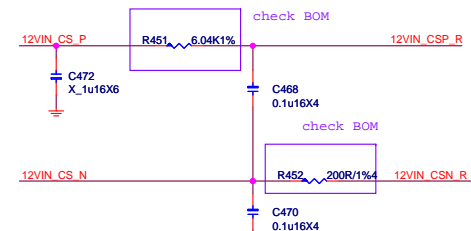


Iripple=30.95A
Vcore 18.101A
VGT 8.457A
VCCSA 4.392A

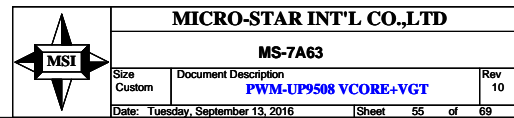
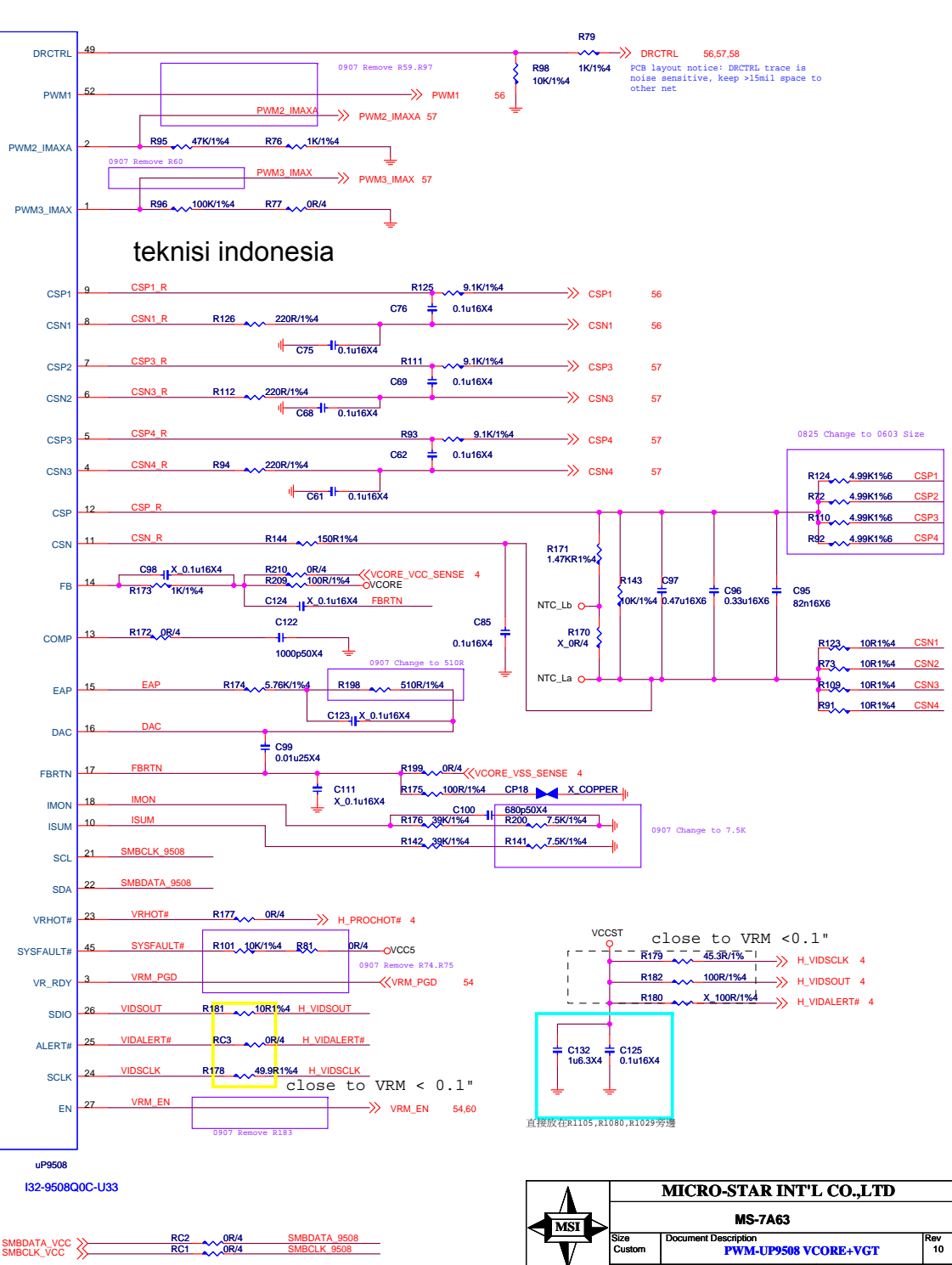
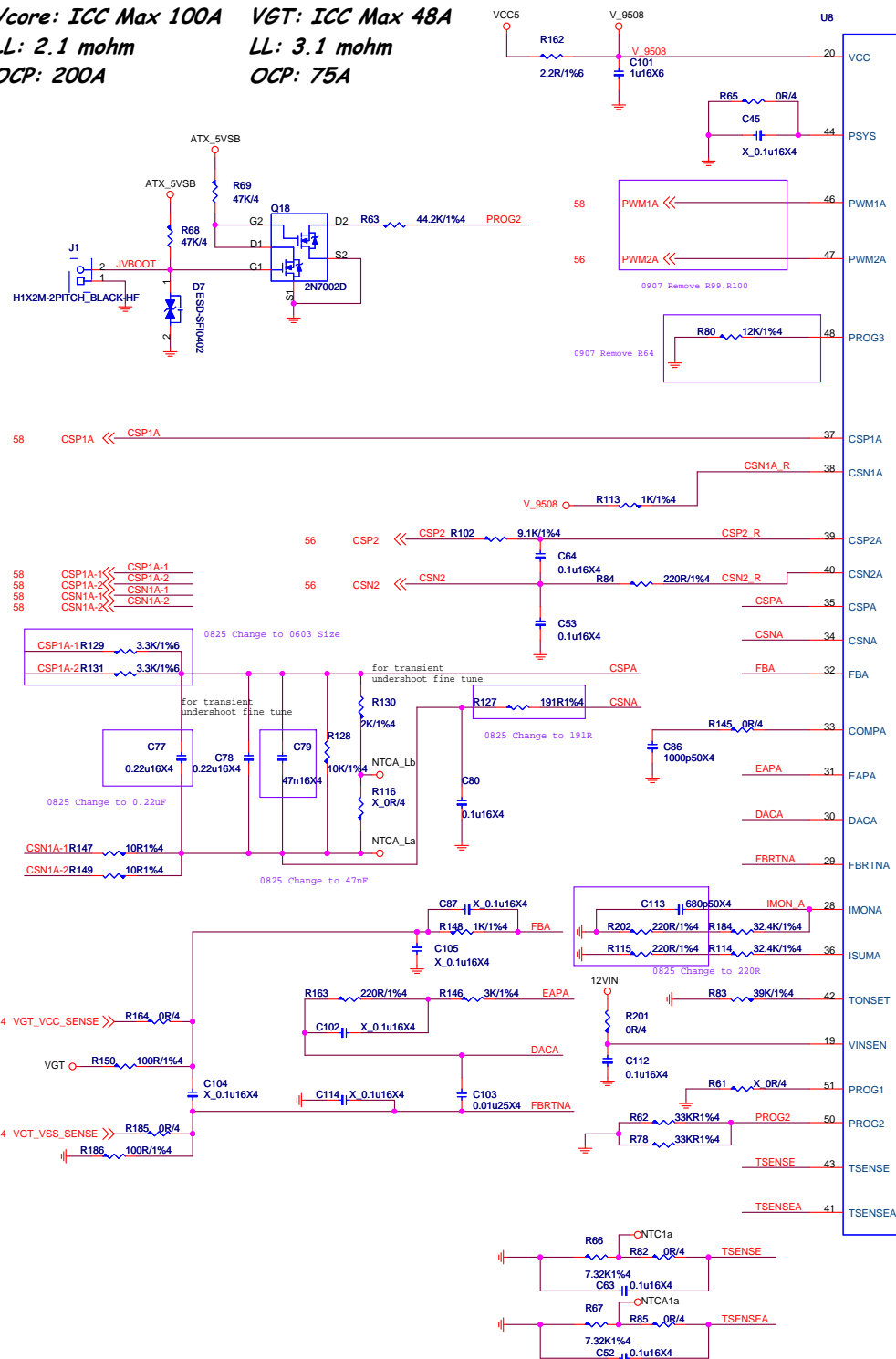
Close to JPWR2

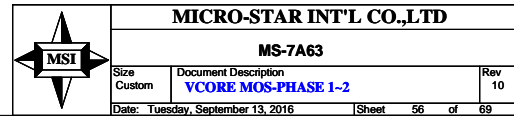


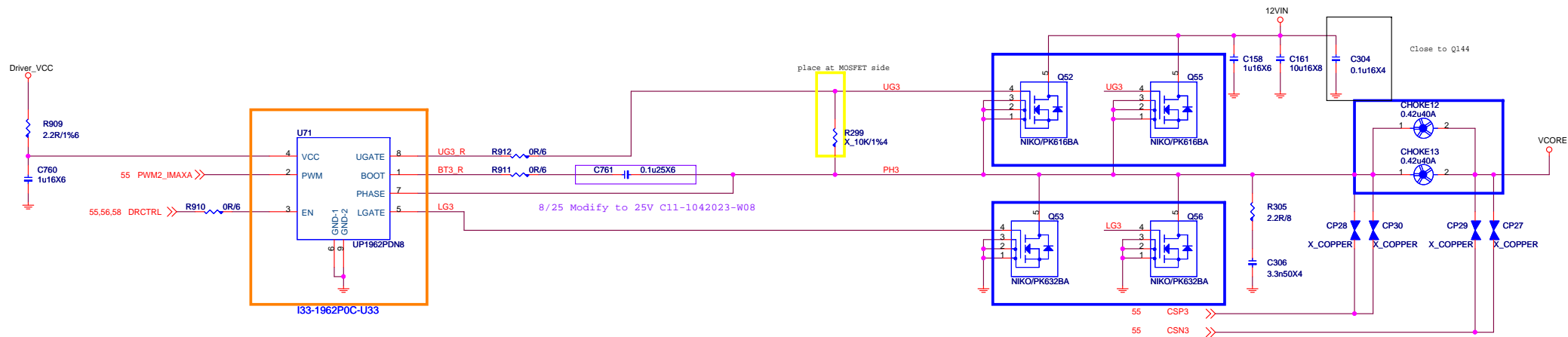
$I_{in} = (V_{mon} \cdot R_{csn}) / (R_{mon} \cdot R_{dc})$
 $V_{mon} = 1.2$
can change OCP trigger level by Rcsn and Rmon



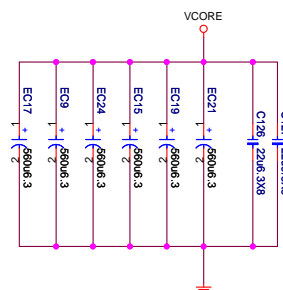
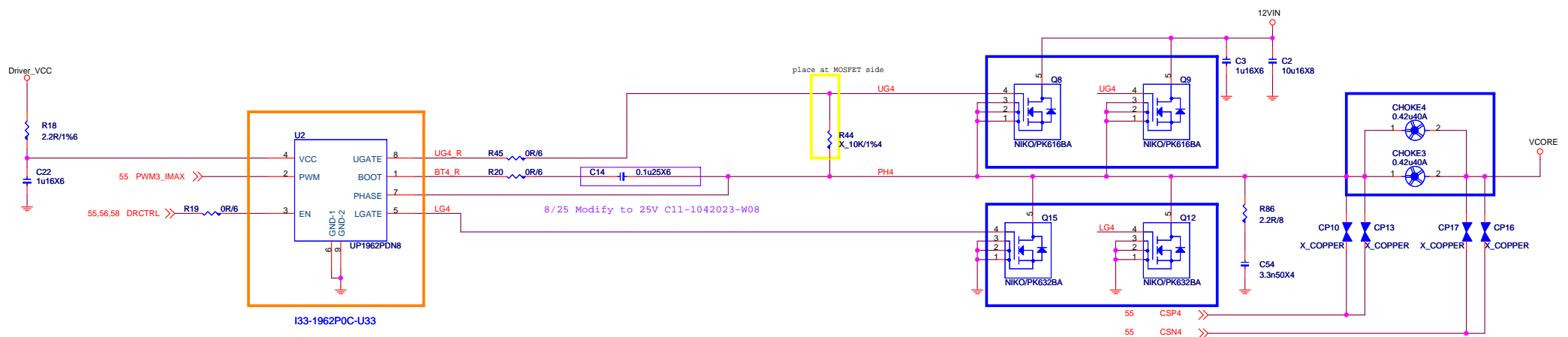
Vcore: ICC Max 100A VGT: ICC Max 48A
LL: 2.1 mohm LL: 3.1 mohm
OCP: 200A OCP: 75A

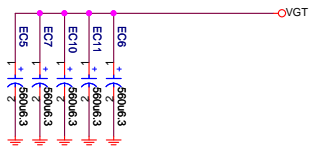
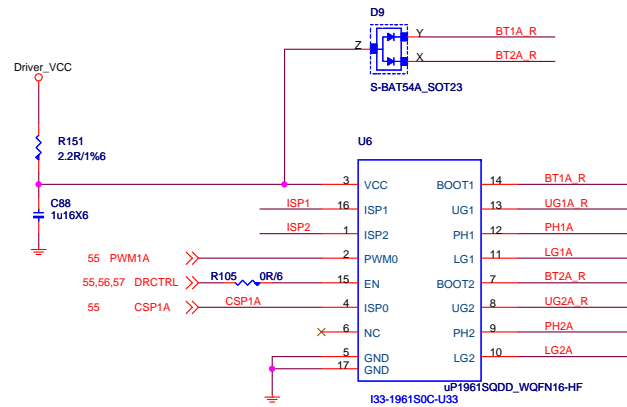




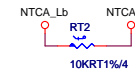


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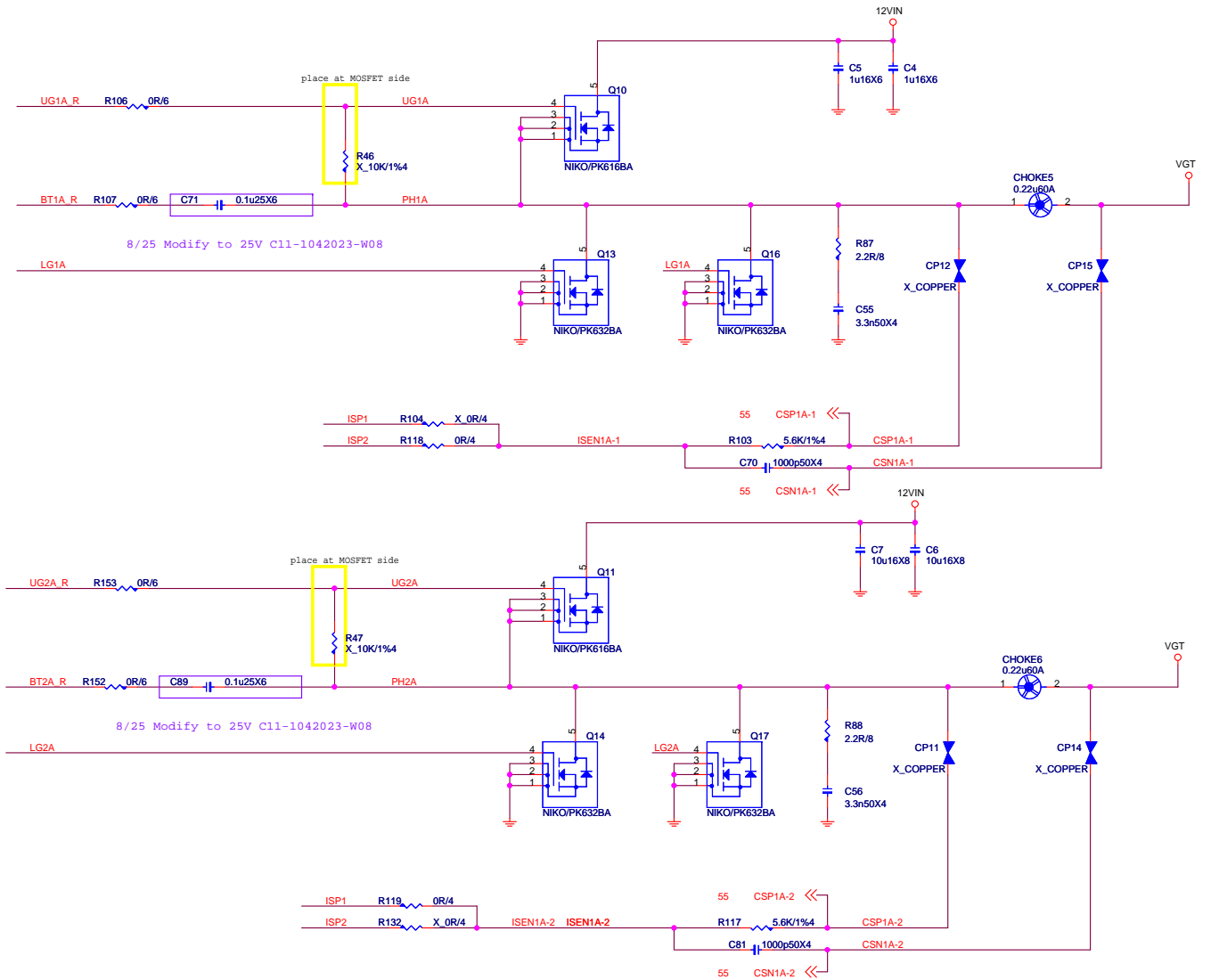
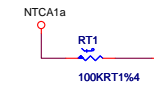




RT2 放在L50與L52中間



RT1放置在VccGT 這組switching power 最熱的地方



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VCCIO

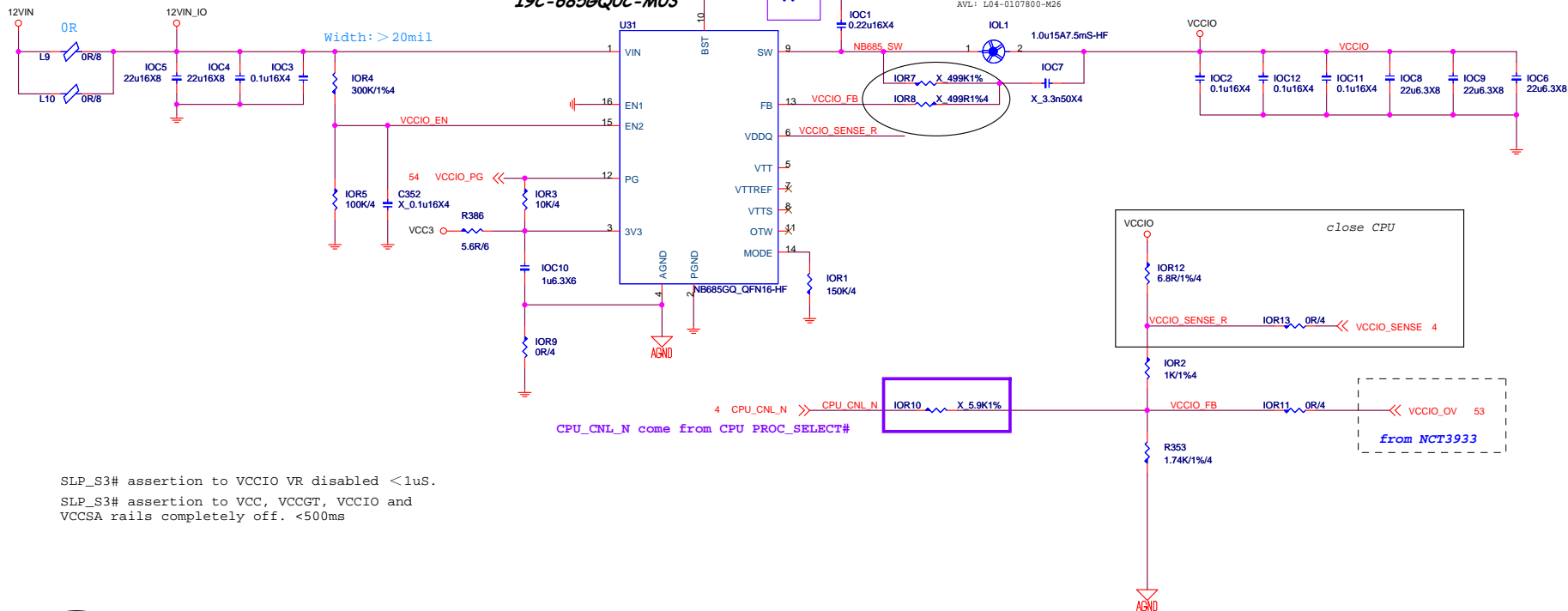
0.95V; 5.5A

support OV=>NB685

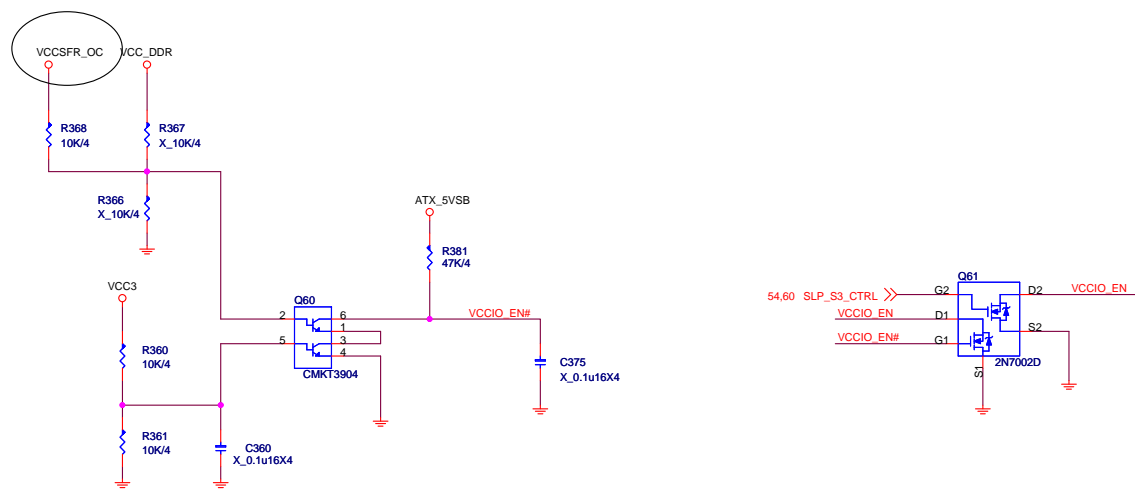
IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

0902 Modify IOR6 to 0603 Size

0.7776uH<L<1.1664uH



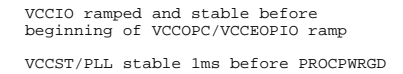
SLP_S3# assertion to VCCIO VR disabled <1uS.
SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off. <500ms



SLP_S3# assertion to VR disabled
max:1us

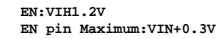
for Gaming3/5, Classic, ECO
and H110

For Cost down VCCST&VCCPLL merge

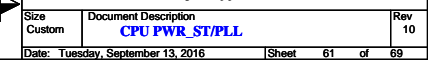


1.2V; 130mA

1.2V; 130mA



2014.08.25 update
S3 have power

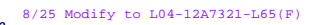



1.2A FOR DDR VTT

$= 9.315 \text{ Kohm}$

use UBIQ MOS need Check

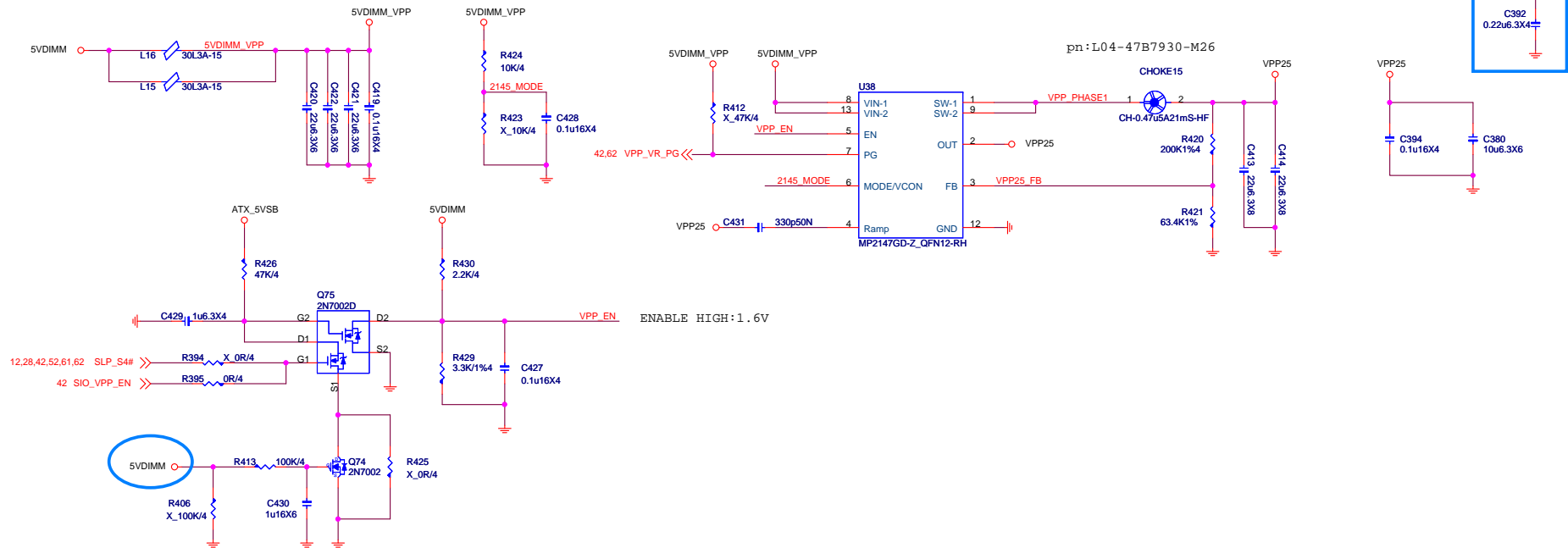
D03-3056M00-U47 : 6.2mohm



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	MS-7A63		
	Size Custom	Document Description DDR4 Power-RT8125C	Rev 10
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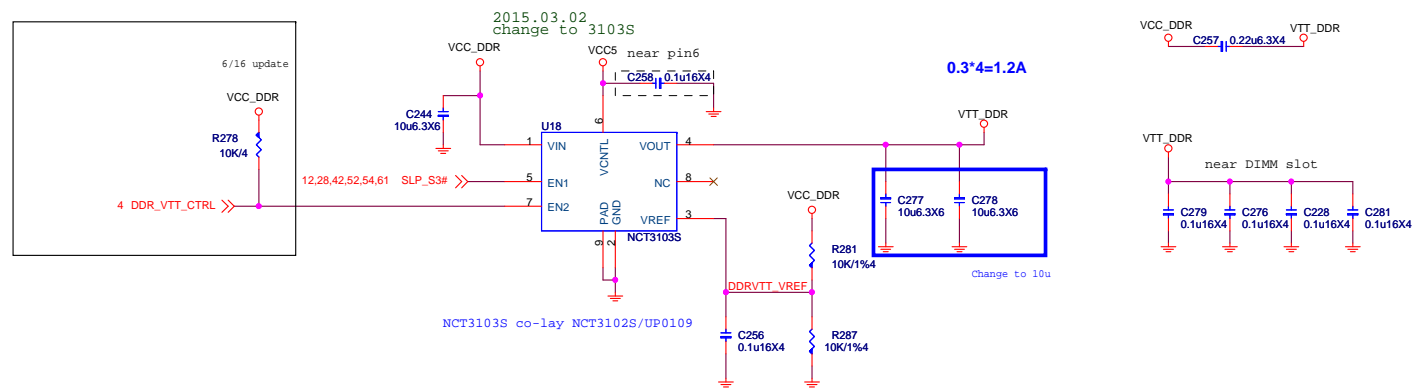
4DIMM :2.24A FOR DDR VPP2.5V

VPP25 Power
2.5V; 2.24A



To make sure VPP EN after 5VDIMM stable

DDR VTT Power



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PCH_1VSB

1.0V; 11.83A

OCP = 17.745A

Rocset = $1.5 * I_{max} * R_{dson}(low) / I_{ocset}$
 = $1.5 * 11.83 * 4.6mohm / 10uA$
 = 8.16K

Rocs: 7.87K, OCP:

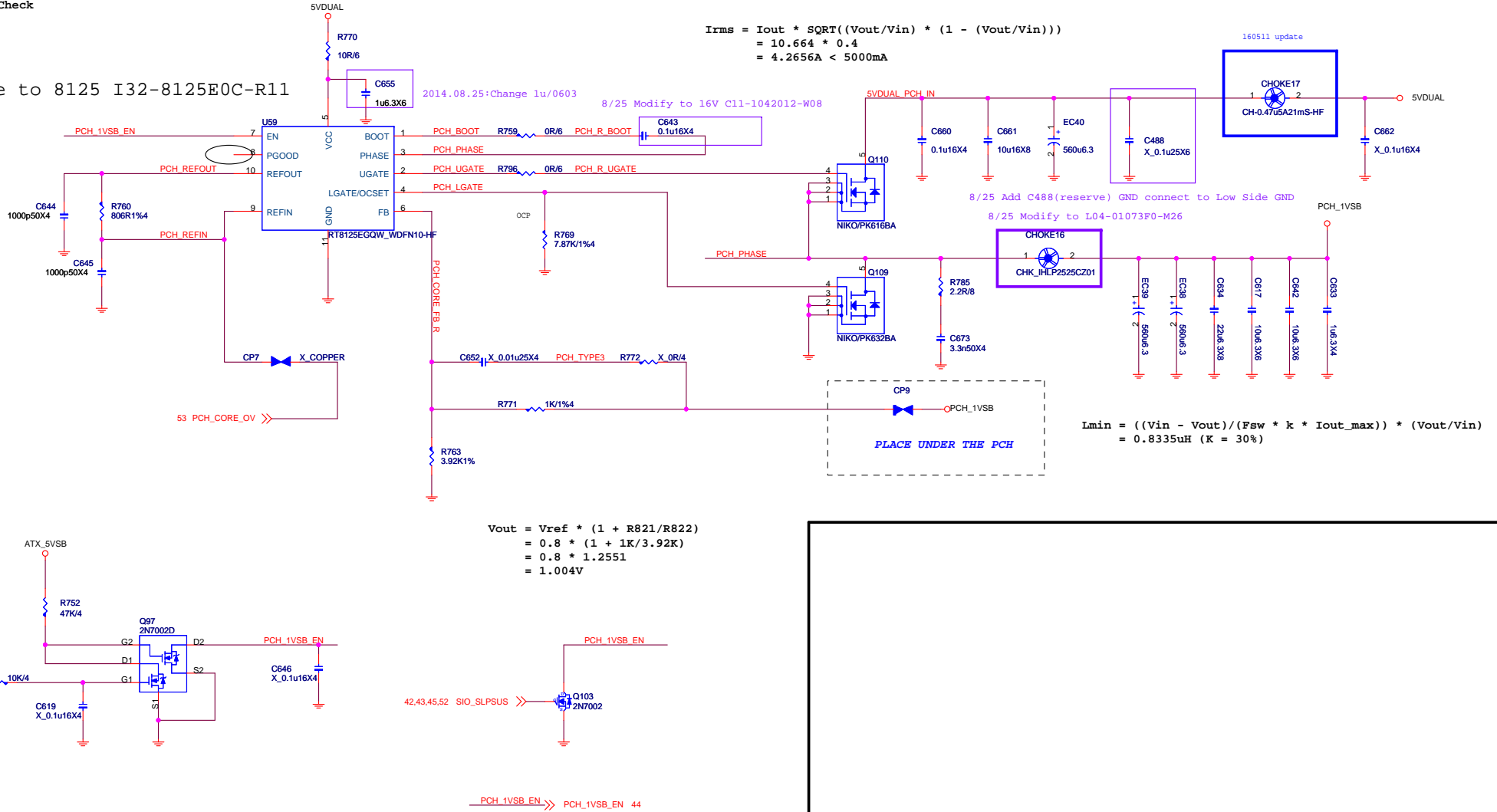
D03-4C05N03-005 : 15.74A

D03-632BA0C-N03 : 17.1A

use UBIQ MOS need Check

$R_{dson}(low) 4.5V$
 D03-3116M00-U47 : 3.6 mohm
 D03-632BA0C-N03 : 4.6mohm
 D03-3056M00-U47 : 6.2mohm

1504 change to 8125 I32-8125E0C-R11



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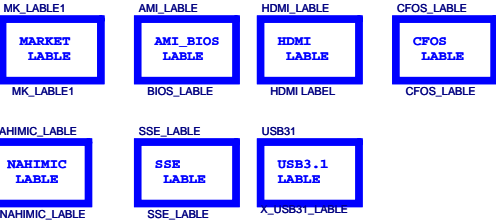
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PCB



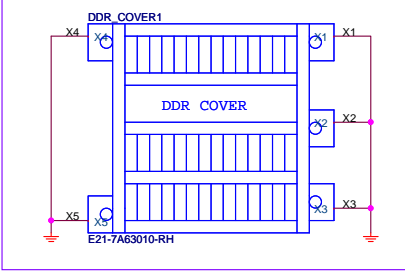
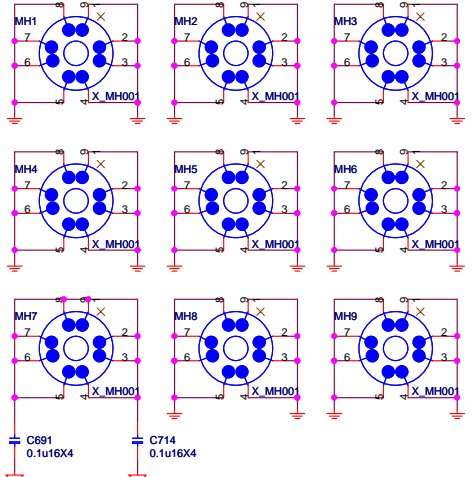
7A63_10
PD0-07A6310-G37
PD0-07A6310-E48



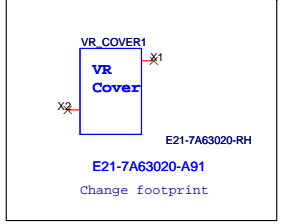
Audio Small Cover



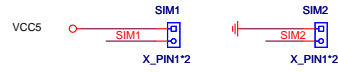
Mounting Holes



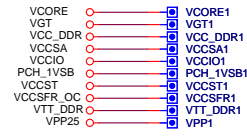
0901 Modify DDR_COVER1 PIN X1.X2.X3.X4.X5 Connect to GND



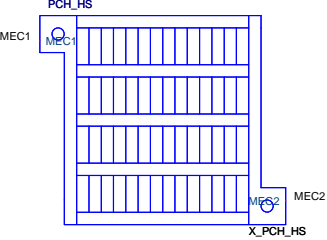
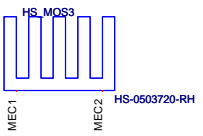
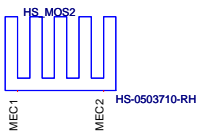
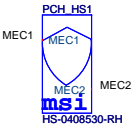
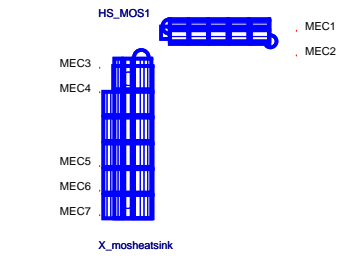
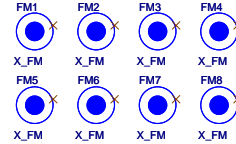
Simulation



Test point



Optical Fiducial Marks-120



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